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Irradiation Impact on Optimized 4H-SiC MOSFETs

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Matthieu Florentin

Director: Prof. Philippe Godignon
Centro Nacional de Microelectrónica

Tutor: Prof. Francesc Guinjoan Gispert
Universitat Politécnica de Catalunya

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Abstract

Silicon (Si) power device' technologies have reached a high maturity level, but current limitations on mechanic, temperature operation and electric performances require to investigate other semiconductor materials that can potentially compete with and overcome those border issues. This is the case of Silicon Carbide (SiC) and Gallium Nitride (GaN) which are becoming serious competitors to the Si due to their superior physical properties. Concerning SiC, the 4H-polytype seems to be the best suitable candidate for high power MOSFETs according to its band gap, electric field strength, electron bulk mobility, and attainable threshold voltage, among others. But still, technological processes must be optimized in order to SiC MOSFETS can compete with their Si counterparts. This is the case of the gate oxidation process. A reduction of interface charge density is required for threshold voltage stability, and further improvements of the interface quality are also needed for high inversion mobility values. Once solved these problems, a path toward new perspectives of high power applications will be opened.

This work is the direct continuation of the Aurore Constant's work. It is focused on 4H-SiC based devices, more specifically on the gate oxidation processes and their behaviour under different harsh environments. Up to now, most of the works carried out were focused on the improvement of the Silicon Dioxide-Silicon Carbide (SiO_2/SiC) interface quality. Solving those problems would allow designing high-speed and low-switching losses MOSFETs. In the past work, the main strength was focused on a new surface pre-treatment and on a gate oxidation process. Results showed improved electrical performances. However, we are convinced that better values can be obtained by optimizing the post-oxidation annealing step, by performing surface counter doping or by performing special irradiation treatments. All the efforts of this work will oriented to the development of reliable SiC MOSFETs with improved electrical parameters, which can operate under harsh environments (like high temperature or proton/electron irradiated environment). Thus, the mains guidelines of this Ph. D. Thesis are in accordance with the following lines:

1. State of the art on various SiC related fields.
2. Electrical characterization processes.
3. Proton irradiation impact on 4H-SiC MOSFETs and charge build-up mechanisms theory at the SiO_2/SiC interface.
4. Electron irradiation impact on 4H-SiC MOSFETs.
5. Gate oxidation and implantation processes optimization.
6. Robustness limit of the improved processes under irradiation environments.

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As a prelude to this Ph.D. thesis dissertation I would like to express my gratitude to the people that contribute to the work reported, and to those that always supported and believed in me.

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Finally, my parents, grandparents, sisters and love receive my deepest gratitude for their support and for having always believed in me.

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List of Symbols and Acronyms

$A_{\_metal\_contact}$	Mercury drop Area [cm^2]
AFM	Atomic Force Microscope
Ar	Argon
BSI	Bias Stress Measurement
BTI	Bias Temperature Instability
C_{DEP}	Depletion capacitance [F]
C_{ox}	Oxide Capacitance [F]
C_{min_dep}	Capacitance in the deep depletion region [F]
CF-PVT	Growth continuous feed – Physical Vapor Transport
CMOS	Complementar Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
d	Distance between two pads of a TLM device [m]
D_{it}	Interface state Density [$eV^{-1}.cm^{-2}$]
DMOS	Double Diffused Metal-oxide-semiconductor
E	Irradiation energy beam [eV]
E’	Defect center
E_c	Conduction band energy [eV]
E_{cs}	Conduction band energy of the semiconductor surface [eV]
E_{cb}	Conduction band energy of the semiconductor bulk [eV]
E_{cr}	Critical Electric Field [eV]
E_{FS}	Semiconductor Fermi level [eV]
E_g	Band Gap Energy [eV]
E_i	Intrinsic Fermi level [eV]
EP	Electrical Parameter
E_v	Valence band energy [eV]
FET	Field effect Transistor
F	Fluence [cm^{-2}]
F_{TH}	Threshold Fluence
GIDL	Gate Induce Drain Leakage
g_m	Transconductance [S]
HTCVD	High Temperature Chemical Vapor Deposition
I_{DS}	Drain-Source Current [A]
$I_{D\_LEAK\_REVERSE}$	Leakage Reverse Drain Current Intensity [A]
$I_{D\_OFF\_STATE}$	Drain-source current in off state [A]
$I_{D\_SAT\_MAX}$	Maximum drain saturation current [A]
IGFET	Insulated-Gate Field-Effect-Transistor
I_{GS}	Gate Current leakage [A]
IRR	Irradiated
IRR+ANN	Irradiated and annealed

JFET	Junction Field-Effect Transistor
K	Boltzmann constant =1.3806504 x 10^{-23} [J/K]
L	Transistor Channel Length [µm]
LPE	Liquid Phase epitaxy
LT	In TLM, it's a typical distance characteristic on which current transfer flow between metal contact and semiconductor [µm]
MOSFET	Metal-Oxide-Semiconductor Field-effect transistor
MESFET	Metal-Semiconductor Field Effect Transistor
MBE	Molecular Beam epitaxy
N_2O	Nitrous Oxide
N_{bulk}	Charge concentration in the oxide bulk [cm^{-2}]
N_{eff}	Effective charge concentration [cm^{-2}]
N_f	Near-interface oxide charge concentration density [cm^{-2}]
N_{fc}	Fixed charge concentration density [cm^{-2}]
n_i	Electron concentration
NI	Non-irradiated
N_{it}	Interface trapped charge concentration density [cm^{-2}]
N_m	Mobile ionic charge density [cm^{-2}]
NO	Nitric oxide
N_{OX}	Oxide trapped charge density [cm^{-2}]
PE-CVD	Plasma Enhanced chemical Vapor Deposition
POA	Post Oxidation Annealing
PVT	Physical Vapor Transport
$POCl_3$	Phosphoryl chloride
q	Basic Electronic charge [C]
Q_{eff}	Effective charge [cm^{-2}]
Q_m	Mobile ionic charge [cm^{-2}]
Q_{ox}	Oxide trapped charge [cm^{-2}]
Q_{it}	Interface trapped charge [cm^{-2}]
Q_t	Traps charge [cm^{-2}]
R_e	End of contact resistance [Ω]
R_c	TLM: Contact resistance [Ω]
R_{in}	Inner Bulk resistance of SiC
R_s	TLM: Square resistance of the active layer out of contact [cm^2]
R_{SK}	Epitaxial resistance under the semiconductor [Ω]
RT	TLM: Global contact resistance of 2 pads measured [Ω]
RTA	Rapid thermal annealing
RTO	Rapid thermal Oxidation
RTP	Rapid thermal process
R_p	Penetration depth of the irradiation beam [cm]

SC	Semiconductor
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
SPE	Solid Phase Epitaxy
TEOS	Tetraethyl orthosilicate
TLM	Transfer Length Method
T_{OX}	Oxidation thickness [nm]
T_{th}	Threshold annealing time [H]
V_{DS}/V_D	Drain-source Voltage [V]
V_{fbth} and V_{fb}	Theoretical Flatband voltage & Flatband Voltage [V]
V_{GS}/V_g	Gate-source voltage [V]
VMOS	Vertical Metal-Oxide Semiconductor
VPE	Vapor Phase Epitaxy
V_{SAT}	Saturation voltage [V]
V_{TH}	Threshold Voltage [V]
V_{TH_NBSI}	Threshold Voltage after a negative bias stress [V]
V_{oxide_br}	Oxide breakdown voltage [V]
V_{TH_PBSI}	Threshold Voltage after a positive bias stress [V]
W	Gate width [μm]
W_m	Metal work function [eV]
Ws	SiC work function [eV]
WBG	Wide Band Gap
Q_{eff}	Effective oxide charge [C]
Z	TLM: contact length [µm]
α	Fitting parameter
ΔV_{TH}	Hysteresis threshold voltage [V]
ΔV_{FB}	Flatband Voltage Hysteresis [v]
εr	Dielectric permittivity [$F.m^{-1}$]
μ_{fe}	Field effect mobility [$cm^2.V^{-1}.s^{-1}$]
μ_{fe_Max}/ μ_{fe_peak}	Peak of field effect mobility [$cm^2.V^{-1}.s^{-1}$]
μ_n	Electron mobility [$cm^2.V^{-1}.s^{-1}$]
μ_p	Hole mobility [$cm^2.V^{-1}.s^{-1}$]
ρ	Target semiconductor density [$g.cm^{-3}$]
ρ_c	Contact resistivity [$\Omega.cm^{-2}$]
ϕ_b	Bulk potential
ϕ_s	Surface potential
σt	Thermal conductivity [$W.m^{-1}K^{-1}$]

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Thesis Outline and Research Objectives

The main purpose of this thesis is to propose a suitable and reliable fabrication process that can improve the main electrical parameters of current Silicon Carbide MOSFETs. Several fabrication experiments have been tested, including implantation, oxidation and irradiation processes. The thesis is divided in three parts with defined objectives. It represents the direct continuity of a previous work. The oxidation previously achieved by oxynitridation helped to improve the SiO_2/SiC interface properties, especially by the use of an efficient surface pre-treatment with hydrogen, and also by nitrogen incorporation during the oxidation process. Both atoms contributed to carbon passivation and reduced interface state density. By optimizing the post-oxidation annealing step, even more successful demonstrations of MOSFETs devices and MOS capacitances characteristics could be obtained. However, the analysed MOSFETs in the previous work were fabricated with an epitaxied body, representing an ideal case. Their electrical characteristics always differed from the real case; i.e., MOSFETs with an implanted body. In the case of an n-channel MOSFET, the overcoming limitation of implanted devices requires a trade-off between several parameters such as energy, dose concentration, type of the implanted atom and inclination of the n-epi-growth of the crystal seed. In this thesis, MOSFETs using the optimum fabrication trade-off so far is presented together with their electrical characteristics. In parallel, important experiments based on irradiated 4H-SiC MOSFETs have been carried out. No less than 23 samples with 6 dices with different gate oxides have been irradiated with protons and electrons at various energies and fluences making a total of irradiated components above 8k. The first conclusion drawn on irradiated transistors was that only MOSFETs whose gate oxide were made up of either a thermally grown oxide by N_2O RTO or by deposited TEOS on the top of the above mentioned thermal oxide provide reliable results. The interface charge build-up mechanisms have been studied, by caring out several standard measurements (transconductance, charge pumping, high-low C-V, etc) but also, by performing time-stress instability on the irradiated MOSFETs. The same irradiated MOSFETs have been annealed several times under different annealing times, and have been measured and compared after each annealing time. This study has allowed observing the effect of charge trapped in the oxide together with the generated interface trap levels after irradiation and post-annealing. In addition, it has revealed that a diffusion process of passivating species through the SiO_2/SiC interface may occur, and can be responsible for the improvement of several device electrical parameters. The irradiation experiment is made of two parts. First, the experiment has been carried out only on the 1st generation of MOSFETs with a relatively poor gate oxide quality in order to put in evidence the irradiation impact. Secondly, the irradiation experiment has been partially repeated on the new designed MOSFETs (2nd generation). In this case, they have been irradiated at various fluences and energies, including 10 samples with 4 dices with the same gate oxide but with different bodies (epitaxied or implanted), making a total of irradiated components above 3k. For specific fluences, the possible mechanism responsible for the improvement or degradation of the electrical parameters has been identified and indexed according to the irradiation fluence and energy.

The main effort has been put in developing reliable SiC MOSFETs with improved electrical parameters which can work under harsh environment conditions, like high temperature or even, proton/electron irradiated environment. This thesis has been split in three main sections, each sub-divided in two chapters.

- ➔ The first section includes a general introduction to the SiC material, and describes the operating principle of MOS capacitor and MOSFET. The MOSFETs main fabrication steps are described in detail and an overview of the problematic regarding the SiO_2/SiC interface is given together with one of the most suitable solution founded to cope with (chapter 1). The electrical characterization methods used in this work to extract the main electrical parameters and to monitor their variation with time and temperature are detailed in chapter 2.

- ➔ The second section is addressed to the deep study of the 1st generation of 4H-SiC nMOSFETs in irradiation conditions. Throughout this part, a special emphasis is put on the threshold voltage and field effect mobility time reliability. A very important chapter (chapter 3) depicts the process irradiation and annealing impacts on Si MOSFETs. In this chapter, the electrical characterization of 4H-SiC MOSFETs using different oxynitrided gate oxides, and irradiated under several fluences and energies with proton particle, is detailed. Benefits and drawbacks of irradiation and post-irradiation annealing processes on MOSFETs having an oxynitrided gate oxide are shown. In addition, the effect of time/temperature post-irradiation annealing is also investigated. From the performed experiments, hypotheses about the irradiation charge build-up and recovery mechanisms within the oxide and at the SiO_2/SiC interface are also suggested. In chapter 4, similar experiments are carried out on 4H-SiC MOSFETs irradiated with an electron beam.

- ➔ In the last section, results on the 2nd generation of nMOSFETs designed with new optimized fabrication processes (p-type implantation or Phosphorous surface counter doping) are shown (chapter 5). In addition, a new gate oxide has been grown on MOSFETs using both implanted and epitaxied bodies. The new fabrication process together with the impact of irradiation and post-irradiation annealing on the MOSFETs electrical parameters are finally discussed in chapter 6.

Finally, the main conclusions of the work are given at the end of this thesis.

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1. NetFiSiC Project

In a first time, it has been possible to carry out this work thanks to the financial support of the NetFISiC project. The project was funded by the European Commission within the 7th Framework Program, Marie Curie actions-European research training network (RTN). Its main objective was to provide Silicon Carbide material of various polytypes (3C, 4H, 6H and 15R), with improved and adequate functional interfaces for getting a step forward in electronic device performances in order to help increasing the competitiveness of European industry concerning electronic devices. Research and effort were dedicated to solve the problems faced by relevant devices like MOSFET and Schottky diodes. Besides, some fundamental research is performed both on the growth aspect and on new and innovating devices. Applications in harsh temperature, high power and high environment are targeted. Emerging technology in SiC is taken as an appropriate tool for study. This shall contribute to long-term strengthening of the European position on a technologically important semiconductor industry. These researches took advantage of MANSiC previous program achievements concerning 3C polytype growth and stabilization in order to propose solutions for material improvement and to provide suitable crystal for electronic devices. The consortium was composed of 12 European partners, including 3 companies, coming from 7 different countries and recognized by their expertise in the field of SiC material and/or related techniques

2. SPEED Project

This project involves 17 companies and research institutions from nine different EU countries. SPEED aims to make a step change in the efficiency of power generation, distribution and transmission through the use of silicon carbide (SiC) - as a higher-performing alternative to silicon - in high-power semiconductor devices. A key contribution of the project is therefore to establish the technology required to produce lower-cost silicon carbide in sufficiently large amounts to compete with silicon. The SPEED project team has already made progress in growing wafers of consistently high quality, using techniques that researchers hope will be industrialized in the future at very low cost. The next challenge is to use the wafers to fabricate circuits and devices. One problem that SPEED aims to solve is the relatively low penetration of renewable energy in the power grid. The next challenge is to use the wafers to fabricate circuits and devices.

Section 1
General Introduction

Chapter 1
SiC MOS devices State-of-the-Art and Objectives

This chapter gives an industrial and general overview on FET components made with silicon carbide. The basics principle of MOS structure and MOSFET, from the architecture to the electrical characteristic, is detailed. Finally, this chapter will also provide the global objective of the work.

1.1 General Introduction to the field

1.1.1 From Silicon to Silicon Carbide

Today, the electronic component market is dominated by silicon (Si). The exceptional advantages of this semiconductor material and its native oxide, together with the well-established and mature process technologies and the industrial effort investment, have allowed Si to cover almost the whole needs in terms of electronic components. However, the current improvement of the Si performances is leading industrials and researchers to reach the physical limit of this material [1]. Although Si is not seen to have competitors in high integration density ICs in a near future, other semiconductor materials must been introduced in the market to overcome Si limitations in applications requiring high voltage, high power, high temperature and high frequency performances. This is the case of Wide Band Gap (WBG) semiconductor materials such as Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond (C), which show excellent theoretical material properties for these applications. Among them, SiC is perhaps the best candidate to compete with Si due to its paramount physical properties (see section 1.2.1), starting material (wafers) availability and process technology maturity. Nevertheless, the development of SiC technologies is currently limited due to a high number of unavoidable difficulties. For example, concerning starting material, difficulties and the complexity linked to the crystalline growth [2] of SiC substrates do not allow the massive production of components. Defect density such as dislocations and stacking faults [3,4] are still important and contribute to limit the production yield. Moreover, to develop metal-oxide-semiconductor field effect transistors (MOSFETs) in SiC technology, some electrical parameters have to be improved. Among them, the field effect mobility (μ_{fe}) has to be increased [5], and the threshold voltage (V_{TH}) has to be reduced and stabilised as well. These improvements are related with the process technology, and some critical steps such as epilayer growth, doping implantation, and oxidation process must be optimised. Specifically, the epilayer growth is currently well mastered on the standard Si-face despite of crystal orientation issues [6] although new strategies for growing low defect density epilayers are still needed. Impurity introduction in SiC is performed by implantation which introduces surface damage that must be recovered for optimal device

performance. This damage recover requires advanced post implantation annealing techniques [7]. Although great improvements in SiC oxidation occurred in this last decade, the SiO_2/SiC interface quality is still poor in comparison with the SiO_2/Si one. Therefore, μ_{fe} of SiC MOSFETs is still very low (in average, μ_{fe} peak values are in the range of 30 $cm^2.V^{-1}.s^{-1}$ in SiC at 25ºC [8] versus 500 $cm^2.V^{-1}.s^{-1}$ for Si [9]). Thus, a lot of effort must be focused on the interface processing technologies to improve the SiO_2/SiC interface quality and to increase mobility.

1.1.2 Introduction to the Field Effect Transistor (FET)

The advent of planar and ICs technologies in the 60's [10-13] made possible to industrially process all type of microelectronic devices. One of the most important inventions in microelectronics is the MOSFET introduced by John Atalla and Dawon Kahng in 1959, and anticipated by Lilienfield, Heil and Shockley [14]. It is nowadays a key component of CMOS technologies and represents more than 70% of the world manufacturing microelectronics. MOSFET belongs to a large family of component named Field Effect Transistors (FETs). These transistors use the electrostatic field effect concept creating a channel at the semiconductor surface, modulating its resistance and controlling the current flowing through it.

Three wide groups of FETs can be distinguished:

- ➔ IGFET (Isolated Gate FET): The field effect comes from a gate isolated from the semiconductor by a thin dielectric layer. In the MOSFET case, silicon dioxide (SiO_2) is used as dielectric.
- ➔ JFET (Junction FET): The field effect comes from a reverse biased pn-junction. This gate bias modulates the width of the channel region and controls the current flow through it.
- ➔ MESFET (MEtal Semiconductor FET): The field effect comes from a reverse biased Schottky (metal-semiconductor) junction. The gate operation is similar to that of the JFET.

1.1.3 MOS Capacitor Operating Principle

A MOS (Metal-Oxide-Semiconductor) is an electronic structure made with a doped-substrate, in our case, 4H-SiC, on which an oxide such as SiO_2 has been grown or deposited. On top of the insulator, there is a metal electrode, which is the gate electrode. The oxide film can be as thin as 1.5 nm. Before 1970, the gate was typically made of metals such as aluminium [15]. After, heavily doped polycrystalline Si has been the standard gate material because of its ability to withstand high temperature processes without reacting with SiO_2. The MOS capacitance is a primary element in a technological characterization. It provides valuable information about the MOS gate oxide thickness, its flat-band voltage, the semiconductor layer doping, the presence of ion mobile charge and also about the interface state density [16]. The role of each parameter is detailed below. Thus, in order to validate a suitable operation of new oxidation process configuration, it is cheaper and faster to test a simple MOS capacitor than fabricating the complete MOS transistor. Moreover, MOS capacitors can be recycled and

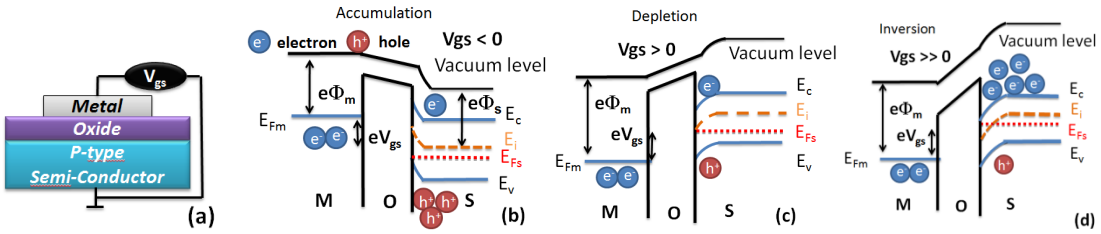

Fig.1.1. The MOS capacitor (a) and the different band structure according to gate-semiconductor bias (V_{gs}) on a p-type semiconductor for $V_{GS} < 0$ (b), $V_{GS} > 0$ (c) and $V_{GS} >> 0$ (d). E_c is the conduction band, E_v the valence band, E_{Fm} the metal Fermi level, E_{Fs} the semiconductor Fermi level, E_i the intrinsic Fermi level, Φ_m the metal work function, Φ_s the semiconductor work function and e the electron charge.

prepared for further manipulations. In [Fig.1.1.a], it is shown a schematic view of the device just described above. The main objective is the fabrication of an n-channel MOSFET hence, the explanation below only consider a p-type MOS capacitor. The operation of MOS capacitance is as follows:

Case Nº1: The MOS capacitance gate-semiconductor voltage is negative ($V_{GS} < 0V$)

When a negative bias is applied to the gate, the electric field at the semiconductor surface displaces majority carriers (holes) toward the semiconductor interface, inducing an upward band-bending. Then, the Fermi level at the surface is closer to the valence band than it is in the semiconductor bulk and the free hole concentration at the surface is larger than in the bulk. The semiconductor surface is equivalent to a p^+-type, which corresponds to the accumulation regime [Fig.1.1.b].

Case Nº2: The Gate-Semiconductor voltage is weakly positive ($V_{GS}>0$)

In this case, the applied voltage is shared between the oxide and the semiconductor surface. The energy bands are downward bended and the electric field sweeps holes toward the semiconductor bulk. Consequently, a depleted region close to the semiconductor interface, where the ionized impurities are not compensated by free carriers, is developed. The energetic distance between the Fermi level and the valence band edge increases near the semiconductor surface. This is the depletion regime [Fig.1.1.c]. The depletion width and, consequently the voltage drop across the semiconductor increases as far as the applied voltage rises.

Case Nº3: The Gate-Semiconductor is highly positive ($V_{GS}>>0$)

As the gate voltage is further increased, the electron-hole pair generation process within the depletion region is also increased. Generated holes are sweep out toward the semiconductor bulk while generated electrons are push to the semiconductor interface as a result of the existing electric field; electrons remaining confined to the interface due to the oxide barrier. The depletion width and the hole-electron generation rate are both increased as the gate voltage increases. In terms of the energy bands, the Fermi level crosses the intrinsic Fermi level, and the conductivity type of the semiconductor surface is changed; i.e., N-type since free

electrons are now majority carriers at the interface (surface inversion [Fig.1.1.d]). However, the electron concentration at the surface is still lower than the ionized impurity concentration (weak inversion). Nevertheless, when the applied voltage accounts for a band bending such as the energetic distance between the Fermi level and the conduction band edge at the surface is equal to that of the Fermi level and the valence band edge at the bulk, the structure enters into the strong inversion regime. In this case, the electron concentration at the surface is equal to the hole concentration in the bulk. Once this regime is reached, any further increase of the applied gate voltage drops across the oxide and, consequently the semiconductor depletion width is fixed. It is worth to remark that electrons forming the inversion layer come from the thermal generation process. In Si technology, the three regimes mentioned above can be detected on the experimental C-V curves.

However, the inversion regime is more difficult to reach in SiC due to its large bandgap. Electron-hole generation process takes place at a much lower rate than in Si, and the inversion layer cannot be formed unless an additional source for increasing the generation (such as a temperature increase or illumination) is provided. Consequently, the MOS capacitor is in the deep depletion regime if the inversion regime is not reached, and the semiconductor depletion width increases with the gate voltage. Typical C-V curves of SiC-MOS capacitors are drawn in [Fig.1.2] where deep depletion is illustrated.

If an additional source for increasing the carriers' generation rate is considered, the inversion layer can be formed. However, this fact will depend on the small signal gate voltage frequency since generated electrons must follow the applied voltage sweep. For high frequencies, generated electrons cannot follow the voltage speed [17].

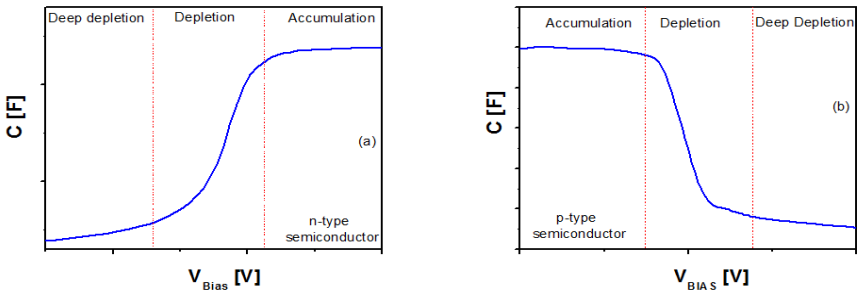

Fig.1.2. C(V) curve for a n-type (a) or a p-type doping (b).

1.1.4 The MOSFET

In the case of an n-channel MOSFET, the structure is built on a p-type layer, in which two highly doped n-zones have been implanted to form the drain (D) and the source (S). The MOS stack is implemented in the region between drain and source [Fig.1.3.a], the control electrode of the capacitor being the gate (G). The source electrode is normally grounded. The current in a MOSFET is made of unipolar carriers (electrons in this case). If the gate is grounded [Fig.1.4.a], no current flow can exist between drain source since the structure behaves like two back-to-back p-n junctions. When a positive gate bias exceeding the threshold voltage is applied [Fig.1.4. b and c], the semiconductor surface becomes inverted (inversion

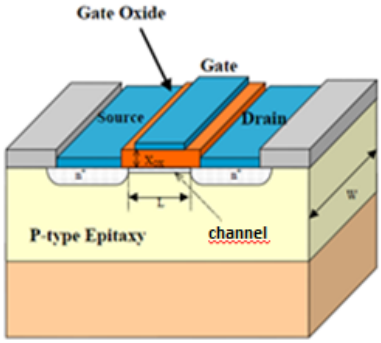

Fig.1.3. Cross section of LATERAL MOSFET transistor

mode), and a conduction channel between source and drain is created. If the drain is positively biased, a current can flow between drain and source through the channel. The channel is created by electrons coming from diffusion from the n^+-source, thus explaining the fact that a MOSFET is a much faster device in comparison with a MOS capacitor.

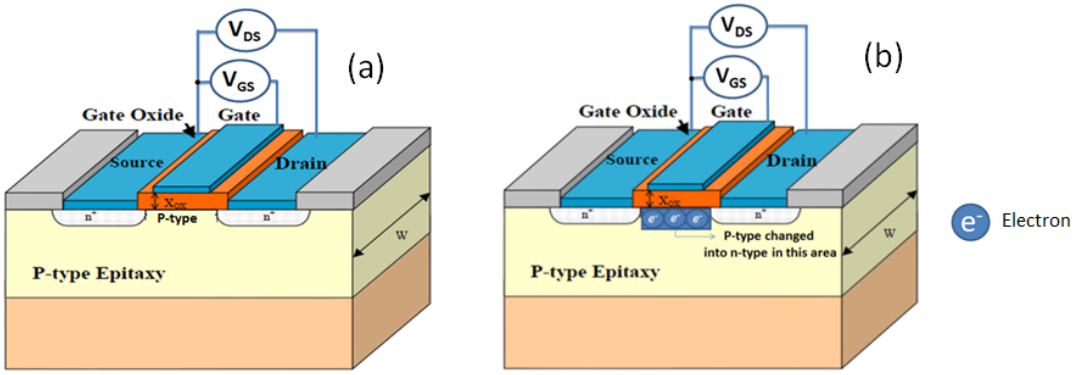

Fig.1.4. Lateral n-channel MOSFET operating principle. V_{GS} = V_{DS} = 0V (a), sub-threshold regime (b) and conduction regime (c).

The typical output and input characteristics are plotted on [Fig.1.5]. As it can be seen from Fig 1.5 a, the output characteristics show a linear region in which current increases with the drain voltage, and a saturation region in which the output current remains constant. The border between the two zones is given by $V_{DS\_SAT} = V_{GS} - V_{TH}$.

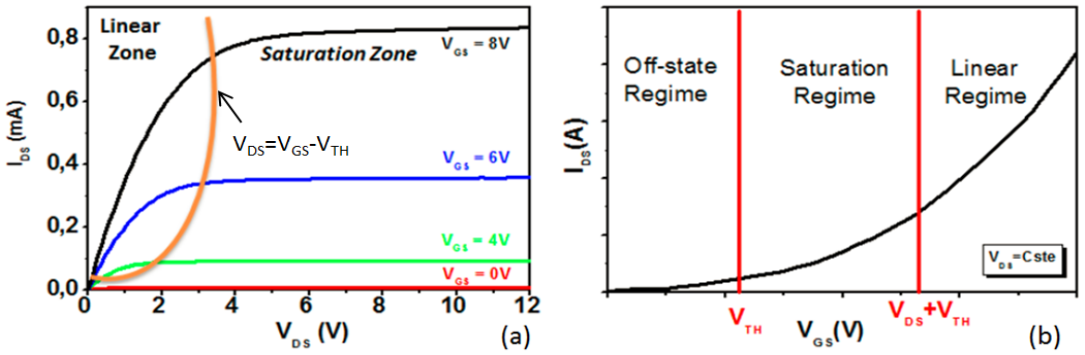

Fig.1.5. I_{DS} (V_{DS}) characteristics for different gate voltages (a) and I_{DS} (V_{GS}) characteristics at V_{DS} constant. V_{DS} represents the drain-source voltage, V_{GS} the gate-source voltage and V_{TH} the threshold voltage.

High voltage power MOS transistors usually have a vertical architecture with source and gate electrodes on the top side of the die and the drain at the backside. This vertical architecture allows increasing the cell integration density (thus maximising the channel width per unit area), Thousands of unit cells are monolithically integrated and provides a high current density capability to the device [18]. This structure gave rise to various types of vertical MOSFET such as VMOS, DMOS, UMOS or Trench MOS [19- 22]. The common drain contact is located at the bottom of the structure [Fig.1.6].

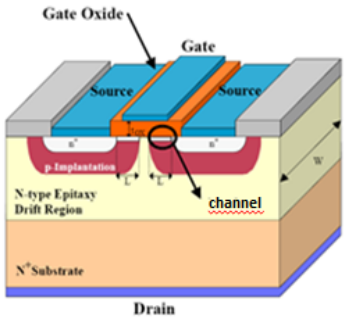

Fig.1.6 Cross section of a vertical MOSFET transistor

1.2. Silicon Carbide for power MOSFETs

1.2.1 The Silicon Carbide and its Properties

SiC-based devices are currently the next generation of power devices to emerge. They are able to work at very high temperature, frequency, and power or in harsh environments [23]. The possibility to get SiC under stoichiometric form was argued by Berzelius in 1824. But only since 1891, Acheson could establish an industrial process for SiC manufacture. SiC first applications were limited to its mechanical properties [24,25]: Harshness for abrasive powders, resistive to high temperature and to chemical products for ceramic protecting coatings. In 1955, Lely discovered a new growth technique which brands the SiC advent [26,27]. The improvement of this technique in 1978 contributed 10 years later to a commercialization of SiC substrate by the world leader CREE and since 2010, by the commercialization of 4H-SiC MOSFETs (1200V/1A). In about 15 years, the diameter of commercial SiC single crystal wafers has increased from 1 inch to 6 inch [28]. Moreover, the controlled growth of high quality epilayers is one of the key issues in the realization of SiC devices. Some years ago, a new striking method to produce ultra-high quality SiC single crystals has been reported [29]. However, some defects like micropipes and dislocations related to the growth of SiC crystal still remain. Indeed, the substrate has to reach its utmost quality with the less defect density as possible. The presence of defects on a wafer substrate reduces the device effective area and the associated yield. Micropipes were initially the prime obstacle for the production of large area SiC-based devices, because they have a direct impact on the breakdown voltage [30]. The density of basal plane dislocations (BPDD) is typically not specified for current commercial wafers as they are of limited importance for unipolar devices. However, this parameter is of crucial importance for bipolar power devices and special material can be ordered with a BPDD of around 2500 cm^{-2}.

This value is then reduced in epitaxy to about 10 cm^{-2}. Nowadays, major effort targets a further improved conversion in epilayer but we also aim at reducing the BPDD of the starting substrate to less than 1000 cm^{-2}.

The term of SiC includes all the carbons and Si stoichiometric forms existing in a solid phase. At room temperature, it does not exist one but various single crystalline structures called polytypes. Each structure is characterized by a different stacking atomic period [31]. One polytype will include n SiC bilayers (planar) and will differ from the others only by its stacking order of the N planes [Fig.1.7]. Among more than 200 indexed polytypes, only three of them have a direct interest for microelectronics applications and one whose properties are still under investigation:

3C-SiC or β−SiC: It is the only cubic polytype (the symmetry is that of the GaAs). Making a lateral transistor with this polytype will bring high channel carrier mobility but with a low breakdown voltage. The number 3 refers to the three bilayer periodicity of the stacking and the letter C denotes the overall cubic symmetry of the crystal. [32]

4H-SiC: It is a hexagonal polytype and it is currently used for vertical MOSFETs' manufacture. It shows the best mobility/breakdown voltage/bulk resistance trade-off. It was earlier found to be energetically most favourable, followed by 6H and 8H, respectively [33]. These higher polytypes are metastable with respect to 3C and, therefore, require non-equilibrium growth conditions.

6H-SiC: It is another hexagonal polytype, but it has the drawback to have a n non isotropic and lower mobility in lateral MOSFET despite of a high breakdown voltage. There are a wide variety of device structures that have been fabricated in 6H, including thyristors, static induction transistors, Schottky diodes, metal-semiconductor field effect transistors and various vertical metal-oxide-semiconductor devices [34-35].

15R-SiC: This is the most mysterious polytype, and its properties are under investigation. It is very difficult to synthetize such a polytype because it needs to be extracted and isolated from the hexagonal structure in a very few percentage (20% in the current maximum case). In order to realize high performance power MOSFETs the results reveal that 15R-SiC should be the best candidate among all current available SiC polytypes [36], but its difficulty to synthesize represents a true challenge for semiconductor technology.

According to its chemical composition, 4H-SiC has some properties between diamond and silicon. The table below [Table.1.1] shows the mains electronic parameters of 4H-SiC, comparing them with those of other polytypes and semiconductors used for power devices. Contrary to the mechanical properties that are especially function of the cohesion energy (low value of inter-atomic spacing between Si-C = 0.188 nm [40] Versus Si = 0.235 nm [41]) some

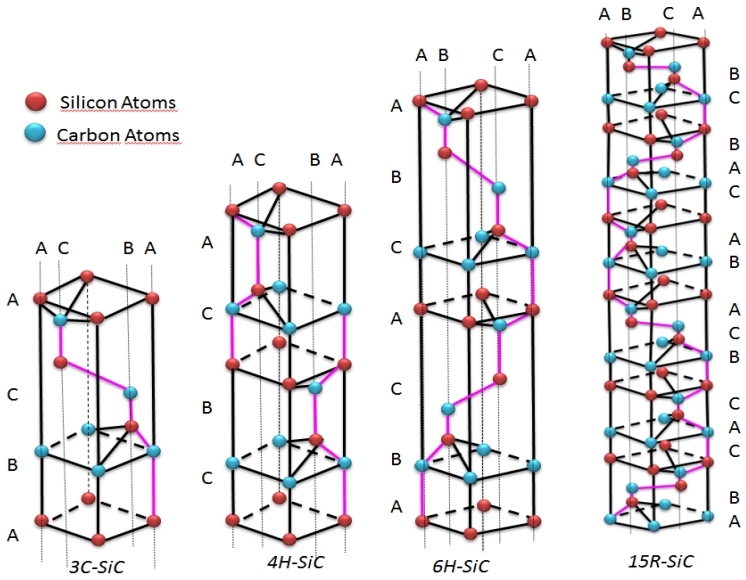

Fig.1.7. 3D Schematic representation of elementary mesh of the main polytypes made with SiC: 3C, 4H, 6H and 15R. Each Hexagon is representative of a bilayer A, B or C following the atom staking (3-D adaptation from [37]).

differences are observed among the different polytypes. In particular, the wide band gap values which can vary from 2.3 to 3.2 eV. At 300K, the 4H-SiC polytype has an intrinsic carrier concentration of only 8.2 x 10^{-9} cm^{-3}, whereas in Si, this concentration reaches 10^{10} cm^{-3}. Moreover, SiC thermal conductivity is three times higher than that of Si. Accordingly, for a same epilayer thickness, a 4H-SiC component will be able to block a higher voltage than a component Si-made. Apart from the 4H-SiC high electron mobility, its higher critical electric field (in comparison with Si) provides a much lower on-state resistance [42]. Hence 4H-SiC is one of the best candidates for high voltage and high power devices. The main advantages of SiC in comparison with Si are summarized in the following [Table.1.2]. An additional advantage of SiC is that among the compound semiconductors, it is the only one that can be thermally oxidized to

Material	E_g(eV) @300K	μ_n (cm^2/V.s)	μ_p (cm^2/V.s)	V_{sat} (cm/s)	E_{cr} (V/cm)	σ_T (W/cm)	ε_r
Si	1,12 (i)	1450	450	10^7	3 x 10^5	1,3	11,1
GaAs	1,4 (d)	8500	400	2 x 10^7	4 x 10^5	0,54	12,9
3C-SiC	2,3 (i)	900	90[a]	2.5 x 10^7	2x 10^6	5	9,6
6H-SiC	2,9 (i)	415	90	2 x 10^7	2,5 x 10^6	5	9,7
4H-SiC	3,2 (i)	950	115	2 x 10^7	3 x 10^6	5	10
GaN	3,39 (d)	1000	350	2 x 10^7	5 x 10^6	1,3	8,9
Diamond	5,6 (i)	2200	1800	3 x 10^7	5,6 x 10^7	20	5,7

Table.1.1. Electrical parameters of the main microelectronic semiconductors. (i) indirect gap, (d) direct gap. From Ref [38-39] [a]Rough estimate. E_g represent the band gap, μ_n and μ_p the hole and electron effective mobility, v_{sat} the saturation velocity of the carriers, E_{cr} the critical electric field, σ_T the thermal conductivity and ε_r the dielectric permittivity.

grow insulating layers and to form high quality SiO_2 layers [43]. These insulating layers are of prime importance in nearly all the SiC industrial applications, like spacecraft, aircraft, automobile, communication or energy distribution, among others.

Properties	Advantages of SiC VS Si	Applications
Electrical	- High electric field - Wider bandgap - High carrier mobility - High saturation velocity	- Power devices - High voltage electronic and sensors - UV and radiation detectors - High frequency electronic compatibility
Mechanical	- High Young module: Resistive to deformation - Harshness	- Mechanic sensors - Protecting coating
Chemical	- Biocompatibility - Inertness	- Chemical and biochemical sensors
Thermal	- High conductivity	- Power devices.

Table.1.2. SiC VS Si

1.2.2 Growth

It represents the first step of the transistor manufacture. SiC occurrence is very rare and it can be found in a natural state only in the moissanite or in some meteorite [44-45]. This is why it is cheaper and practical to synthetize the SiC starting from Si. In order to do so, some techniques are used, like, Physical Vapor Transport (PVT) [46-48], High Temperature Chemical Vapor deposition (HT-CVD) [49] and growth continuous feed – Physical Vapor Transport (CF-PVT) [50].

1.2.3 Epitaxy

In order to fabricate a MOSFET, there are two possible options: The first one consists in an epitaxial layer (or epilayer) growth. The epilayer grown on substrate will determine the nature and the quality of the conduction channel. In the second option, an implantation can be realized in order to change the doping without acting on the transistor thickness. To achieve these goal, a very low contamination rate is required.

The epitaxial growth is one of the most important techniques to fabricate various 'state of the art' electronic and optical devices. Modern devices require very sophisticated structures, which are composed of different thin layers. Quality, performance and lifetime of these devices are determined by the purity, structural perfection and homogeneity of the epitaxial layers. The epitaxial crystal growth has to account for the surface flatness and interface abruptness, which depend on factors like the epitaxial layer growth method, the interfacial energy between substrate and epitaxial film, as well as the growth parameters: thermodynamic driving force, substrate and layer mismatch, substrate misorientation, growth temperature, etc… One can be distinguished between the "*homo-epitaxy*" that consist in a growth of two crystals with identical chemical nature, and the hetero-epitaxy in which crystals are coming from two different

chemical species [51]. In 1983, a major step forward was achieved by Nishino, Powell, and Hill who made the first heteroepitaxy of SiC on Si [52]. In 1987, this technique was further improved and the next stage of SiC evolution started with the high-quality heteroepitaxy performed at low temperatures on off-axis substrates using " the step controlled epitaxy".[53].

In most of the cases, the epitaxy is mainly made by chemical Vapor Deposition (CVD). This technique remains the most performing one even a lot of techniques can be used (VPE, LPE, SPE, MBE etc…) to grow epilayers [54]. The wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber. Commercial SiC epilayers are grown by the CVD technique, which has a growth rate around 5µm/h but thick epilayers are difficult due to instabilities during long growth period. However, tremendous improvements have been experimented on epi growth rates obtained by CVD, either using chlorinated precursors or with the standard SiH_4-C_3H_8 system done in the past few years. Nowadays, growth investigation is oriented toward:

- Growth and thickness speed increasing, Uniformity improvement, Residual doping decreasing, defect reduction (micropipes, stacking fault etc…) and other crystalline orientation growth mastering.

For an efficient emission or detection of photons, it is often necessary to constrain these processes to very thin semiconductor layers. Also, the growth angle of an epitaxial layer is crucial for SiC substrate, because it has a direct impact on the surface roughness, and on the electrical characteristics of the MOSFET [55-56]. Then, the less inclined growth, the better the surface roughness but the more complex technique has to be used.

1.2.4 Implantation doping

After growing the epilayer, the following step in order to fabricate a lateral MOSFET structure is the formation of wells by ion implantation. They will be the drain and the source of the transistor. These wells will be highly doped n-type or p-type. After such an implantation the implanted atoms predominantly occupy interstitial lattice sites usually not electrically active [57] Then, they will be electrically activated by bringing them a high energy by using a rapid thermal process. Vacancies generated at elevated temperature (1200°C) facilitate the movement of implanted species from interstitial to substitutional lattice sites while amorphization damage from the implantation process re-crystallizes. In a relatively rapid process, the peak temperature is often maintained for less than one second to minimize unwanted chemical diffusion [58].

The implantation doping It allows a well-controlled distribution of the doping species in terms of concentration and depth. However, a main issue remains, which is related to the damage produced in the crystal lattice. The realization of an n-MOSFET structure requires a hole-doping implantation, carried out by masking. Thus, some parameters have to be optimized such as implanting dose, SiC temperature during implantation, defect recovering anneal and the doping activation after implantation. Once the n/p wells are formed by using mainly phosphorus

or nitrogen as donors and boron, and aluminium or gallium as acceptor [59-60], it can be proceed to the gate oxide manufacture.

1.2.5 Oxidation of the Interface

In the process technology context, the insulating layers like gate oxide or passivation layer are necessary to form the MOS gate controller to prevent from leakage within the periphery (field oxide). In comparison with its competitor's materials, SiC has the unique potential to be thermally oxidized for forming a silicon dioxide silicate (SiO_2) film. The use of this insulator as a gate oxide is the basic of power MOSFET development. The oxidation process is controlled by the equation (1.1) [61]:

$$SiC + O_2 = SiO_2 + C \text{ and/or } SiC + \frac{3}{2} O_2 \quad (1.1)$$

The carbon atoms left in the oxide will also be determined by the reaction [62] (1.2):

$$2C + O_2 \leftrightarrow 2CO \text{ and } SiC + 2CO \leftrightarrow 3C + SiO_2 \quad (1.2)$$

In practice, SiC growth oxidation rate is lower than Si and needs a temperature over 900ºC in oxygen or H_2O vapor atmosphere. Its oxidation rate depends on several factors such as the SiC polytype, doping or crystallographic orientation. Several oxidation process techniques have been considered and described below:

Deposited Oxide

The most popular method to get a thicker oxide is to make a CVD deposition. This oxide deposition does not consume any SiC. Therefore, it does not generate extra interface charges. Different techniques exist in order to deposit those insulating layers like PE-CVD [63] or LPCVD [64]. Regarding this deposition technique, the oxidation layer is carried out at low temperature (600ºC) by CVD using Tetra-EthyOxy-Silane (TEOS) as a precursor gas. At elevated temperatures (>600 °C), TEOS converts to silicon dioxide (1.3).

$$Si(OC_2H_5)_4 \rightarrow SiO2 + 2(C_2H_5)_2O \quad (1.3)$$

This deposition is followed by an annealing in nitrogen atmosphere around 700ºC [65] in order to densify the oxide layer.

Thermal Oxidation

The physical phenomena that enter into account are totally different from the oxide deposition. Indeed, in the case of the thermal oxidation, a high temperature chemical reaction occurs between oxygen and SiC. The SiO_2 layer is grown consuming Si atoms from the SiC surface. The oxidation can be carried out in dry atmosphere (100% of O_2) or in wet atmosphere (with H_2O vapor). Moreover, it seems that the wet oxidation may show a density of defects lower than the dry one [66]. For this thesis, Rapid Thermal Process (RTP) furnace is used to proceed to the gate oxidation of the MOSFET, yielding a very different type of oxide. The furnace, allows

achieving very fast and high quality oxide layers whose interface state density are comparable to the best reported in the literature [67], meaning that the number of traps at the SiO_2/SiC interface is relatively low. A short description of the process is detailed in 1.2.4.

1.2.6 Identification of the SiO_2/SiC Interface Traps

The oxidation process is problematic for all SiC polytypes, no matter the oxidation process. One of the biggest issues that researchers have to deal with is the carbon atoms presence at the interface, since it is related to its high defect density. These defects were put in evidence at the end of the 90's [68] and they are responsible for the low channel mobility of 4H-SiC MOSFETs. They lead to much higher on-state resistance than expected from bulk material properties [69]. These defects give rise to traps that can be either donor-like or acceptor-like. A donor trap releases an electron when it moves from below to above the Fermi level. Donor traps are neutral when fulfilled by an electron, and positively charged when empty. An acceptor trap captures an electron when it moves from above to below the Fermi level. Acceptor traps are neutral when empty, negatively charged when fulfilled. The different types of charges are described below and depicted in [Fig 1.8.a]:

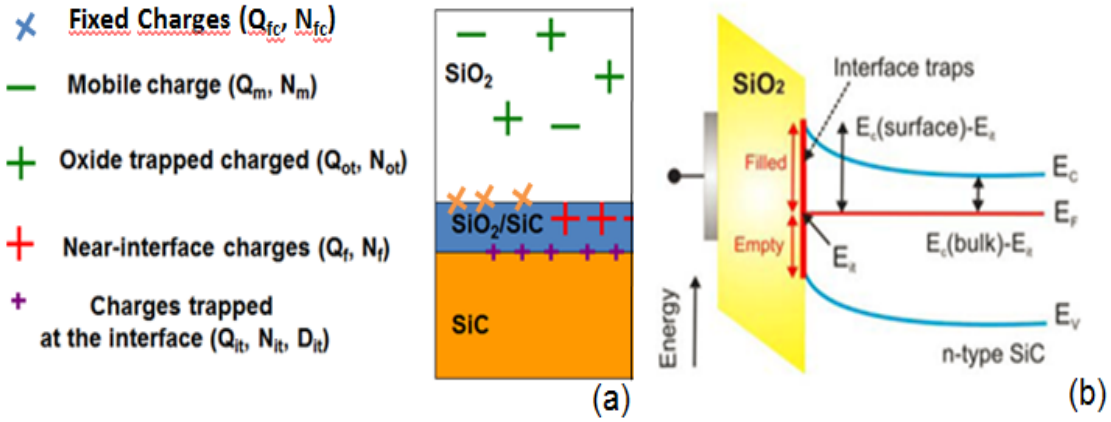

Fig.1.8. (a) Different charges and their locations in the MOS structure ([70]) (b) Energy levels at the oxide/n-type SiC interface in depletion and energetic location of interface traps [71].

Ion mobile charges

These light charged ions are generally atoms introduced in the oxide during the manufacture process, mainly due to ion impurities such as Na^+, K^+ and Li^+ [72]. Some of these are incorporated in a positively charged ionic form, which are mobile within the oxide in presence of an electric field, introducing undesired instabilities in the electrical characteristics of the devices [73]. Mobile charges can be reduced by an efficient surface conditioning process prior to the oxidation and by a post-oxidation process.

Oxide trap charges

These are the result of trapping carriers inside the oxide. The oxide traps are associated to defects created either by impurities, radiation damage in the oxide layer, or by hot carriers injection. They are usually neutral and become charged when electrons or holes are trapped. They induce a shift of the MOSFET I_{DS} (V_{GS}) curve toward the left or the right depending on the charge type. Moreover, a weak gate leakage can enhance the charge trapping. Their presence also produces a hysteresis in the C(V) curves. Therefore, C(V) hysteresis measurements allow calculating the oxide and ion mobile trap charge densities (Section 2.1).

Interface fixed charges

Dangling bonds are present at the SiC surface before the oxidation step due to the periodicity rupture of crystalline lattice. Depending on the environment, dangling bonds may attract some random free atoms potentially able to introduce additional allowed energy levels within the bandgap. When the flatband voltage is shifted toward a positive voltage range, the fixed charges are negative, while they are positive if the flatband voltage is shifted toward a negative voltage range. The presence of the fixed charge is detected by the C(V) measurement, because they depend on the voltage difference between the flatband voltage of the hysteresis return and the theoretical flatband voltage, and also on the flatband voltage shift (ΔV_{FB_IL}) of the interface ledge [Fig.1.8.b] [74].

Interface and near interface oxide traps (NIOTs)

They are interface traps that can be fast charged with charges coming from the semiconductor. They are mainly due to the surface carbon layer and existing impurity atoms. These traps are electrically linked to the semiconductor and can be charged or discharged, depending on the surface potential value [75]. When a voltage is applied to a MOS capacitor, the valence and conduction bands bend up or down, while the Fermi level remains constant, and the interface trap energy levels can be either above or below the Fermi level; thus changing the trapped charge value. A change of interface trap charge density results in a variation of the capacitance, altering the C(V) curve of an ideal MOS device. Concerning the SiO_2/SiC main interface traps, interface and near interface oxide trap charges are the most harmful ones and the most numerous as well. Currently, with the recent progress in SiO_2/SiC interface, they can range between 10^9 up to 10^{13} eV^{-1} cm^{-2} near the conduction band for the most recent oxides grown on n-type semiconductor [76]. Their presence is reflected by a hump in the C(V) curves [Fig.1.9]. In order to better understand the role of the mentioned traps in the C(V) curves, a short description of the C(V) hysteresis shape is necessary. The description is based on the C(V) curves shown in [Fig.1.9.b] following the sequence A→B→C→D→E→A.

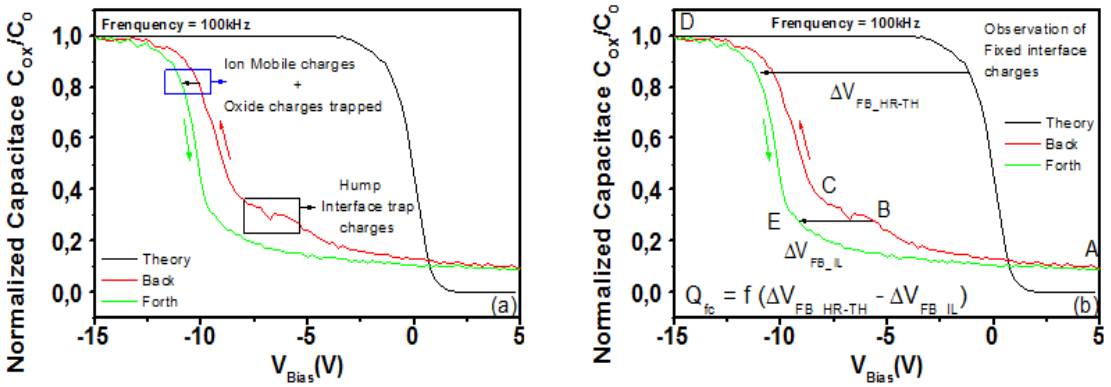

Fig. 1.9. Example of a C(V) electrical characteristic of a p-type MOS structure showing the impact of the different interface traps located at the SiO_2/SiC interface, including the ion mobile charges, oxide charges trapped and interface traps charges (a) and fixed charges (b). ΔV_{FB_HR-TH} is the flatband voltage difference between the experimental flatband voltage of the hysteresis return and the theoretical flatband voltage. ΔV_{THFB_IL} is the flatband voltage of the interface ledge.

A→B: At point A, the MOS capacitor is in deep depletion. Therefore, there are few electrons thermally generated that can be eventually trapped by the existing interface states. Because deep interface states are mostly donors [74], their nature due to the electron trapping is neutral. By decreasing the gate bias, electrons are being less and less numerous, and holes start to accumulate at the semiconductor surface for negative gate biases.

B→C: The observed hump is due to the hole capture by interface state located in the bandgap. As S.Berberich explained in his work [75], within a narrow range of surface potential, most of the neutral surface states can be charged by hole capture. This hole capture associated with the surface hole accumulation due to the gate negative bias provokes a fluctuation of the capacitance whose amplitude depend on the amount of tunnelled positive charges to the SiO_2 layer, at a given surface potential.

C→D: The hole accumulation is increasing. At point D, the deep traps (that were capturing electrons in the deep depletion regime) keep on capturing more holes, becoming positively charged. Moreover, both ion mobile charges moving due to the applied bias and fixed charges can also trap holes.

D→E→A: In this region, the charge state of the interface states is positive. However, once holes have been captured at interface states, they cannot be thermally emitted to the valence band at room temperature. The voltage shift observed between B and E is due to the interface state charge difference.

1.2.7. Oxidation under RTP: A Threefold in-situ Process

The key point in overcoming these interface state issues lies on a nitridation process. It is an oxidation process in a nitrogen atmosphere, NO or N_2O. During the oxinitridation process, nitrogen atoms passivate the carbon's dangling bonds [77]. However, the required thermal budget is important (typically 0.9 nm oxide per hour at 1050º C). In the case of the 4H-SiC polytype, the interface state density ranges from 10^{14} to 10^{15} $eV^{-1}.cm^{-2}$ when no special treatment is applied [78]. Thus, most of the investigation about SiC oxidation processing has consisted into reducing those traps as much as possible. Oxinitridation under a Rapid Thermal Process (RTP) has been one of the chosen solutions to face the interface state charge issues. Three steps have been established in order to perform a good oxidation process: surface pre-treatment, oxinitridation and anneal. Recently, it has been demonstrated the efficiency of the oxidation process under RTP furnace, which is a furnace that utilizes UV rays for reducing the carbon atom amount before oxidation [79]. Oxidation processes with this type of furnace allows obtaining excellent oxide qualities, with a low $D_{it,}$ increasing μ_{fe} [80]. 42.5 nm of oxide can be grown in 20 minutes (including post-oxidation anneal) [Fig.1.10], whereas it takes several hours in a conventional furnace [81].

The most efficient oxidation process used for MOSFETs fabrication consists in a threefold in-situ process. Before oxidation, the wafers are submitted to an HF cleaning. They are loaded into the RTP furnace afterward. The first step consists in a surface pre-treatment cleaning by H_2 at 800ºC for 120s [82-85], since not only UV-ozone can contribute to surface improvement of the SiO_2/SiC interface, but also various hydrogen treatment under different form (wet chemical [86-87], plasma [88-92] or annealed in CVD reactor [93-96]). Next is the oxinitridation under N_2O at 1050ºC for 10 min. During the oxinitridation, the nitrogen atoms come to partially passivate the carbon dangling bonds, creating several C-N bonds [97]. The well-known effect of nitrogen passivation leads to the creation of a bonded Si-C-O-N interlayer (SiO_xN_y interlayer with the presence of passivated SiO_xC_y complexes) [98]. NO diffuses through the SiO_2/SiC interface, dissociates and penetrates the near-interface region. In the last decade, nitrogen oxinitridation has been recognized as one of the best efficient ways to grow a high oxide quality on a SiC wafer, because of its simultaneous effects: Oxidation, interface trap passivation and carbon removal at the interface. Thus, the interface state density (D_{it}) can be successfully reduced. Nevertheless, it has been shown that nitridation process requires a very high thermal budget. Reports about nitridation process using N_2O have been mostly limited to above 1200 ºC [99], so far because 4H–SiC is oxidized in N_2O at such high temperature. In order to increase the oxidation rate and control the oxide formation in a N_2O ambient, the RTP furnace is a reliable solution [100]. Once the oxidation is carried out, crystalline lattice structure is in a disorganized state because of the changes provoked by the introduction of new species (mainly nitrogen and oxygen atoms). Thus, the crystalline reorganization and stabilization is very important. It would be worth if the species used for the annealing could contribute to further decrease D_{it}. High temperature annealing in NO gas after a thermal oxidation in O_2 has been firstly recognized to be effective to reduce D_{it} [102]. Then, *Keiko Fujira et al* [103] were sure

about the benefit of the N_2O nitridation on interface traps, since N_2O is preferable to NO for safety reasons. Argon and hydrogen anneals were also experimented by S. *Suzuki et al.* [104]. Results showed that even if argon could reduce D_{it}, hydrogen was more efficient, because of temperature limitations (it has to be done around 800ºC). *Dai Okamoto et al* [105] showed the positive effect of the phosphoryl chloride ($POCl_3$) and boron (B) [76]. They succeeded in reducing the interface state densities down to 9.10^{10} $cm^{-2}.eV^{-1}$ with $POCL_3$ in 2010 and down to 3.10^9 $cm^{-2}.eV^{-1}$ with B diffusion on n-type MOSFETs in 2014. The use of Phosphorus as a component for surface counter doping is given in chapter 5, section 5.2.1.

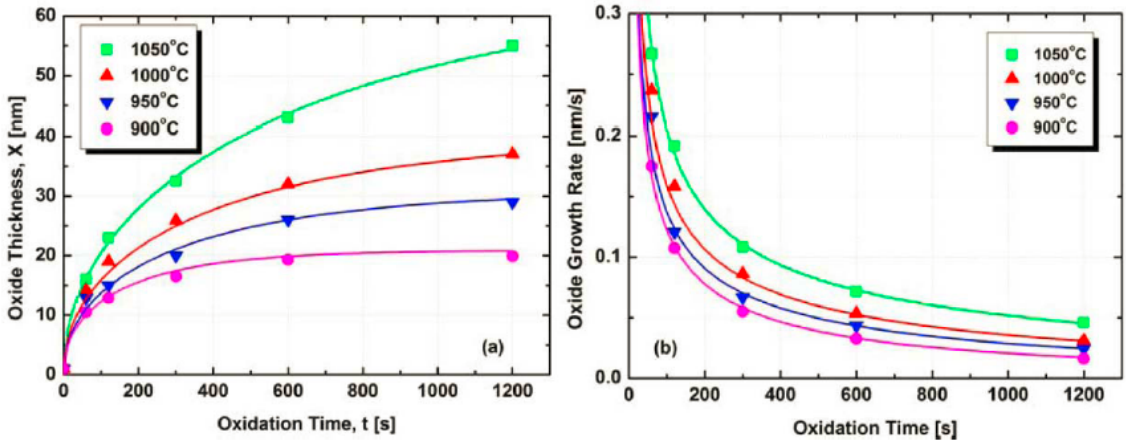

Fig.1.10. Example of gate oxide thickness (a) and oxide growth rate (b) as a function of oxidation time and substrate temperature for rapid thermal oxidation in N_2O of (0001) p-type 4H-SiC [101].

1.2.8 Process Technology

Despite all SiC advantages previously mentioned, there is one main issue to be solved: The high interface state density induces low field electron mobility in the inversion channel. These issues reveal the importance of various manufacture steps, including substrate growth, epitaxy, implantation and oxidation. A SiC MOSFET manufacture includes a certain number of key-technological steps described in the [Fig.1.11] below:

In the case of a SiC MOSFET, the important issues are:

- ➔ SiC substrate manufacture (because SiC is very rare to find in a natural state).
- ➔ Epitaxy with the appropriate mastering of the required doping level.
- ➔ Implantation and post-implantation annealing.
- ➔ Oxidation and interface state defect reduction.
- ➔ Metallization and contact resistance reduction.

In [Fig.1.11], the mask used for MOSFET fabrication is shown. The mask set consists of 7 levels as follows:

1. Plasma etch of alignment patterns.
2. P-well implant mask.
3. N^+ - implant mask for the definition of source and drain of the MOSFETs.
4. Gate active area definition.
5. Contact opening.
6. Contact metallization pattern.
7. Gate metallization pattern.

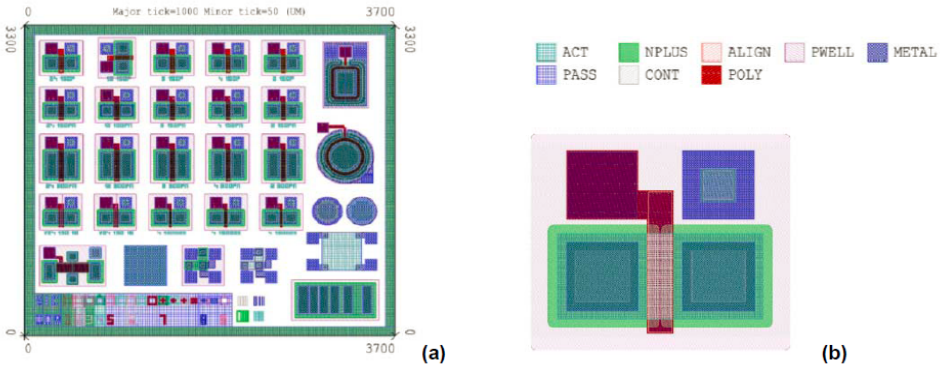

Fig.1.11. Mask layout showing a monitor chip (a) and the layout for a lateral MOSFET (b)

The layout shown in Fig. 2.3.a includes the following devices:

- ➔ 5 MOSFETs with L/W (μm) = 24/150, 12/150, 8/150, 4/150, 2/150
- ➔ 5 MOSFETs with L/W (μm) = 24/300, 12/300, 8/300, 4/300, 2/300
- ➔ 1 rectangular MOSFET with W = 1 mm; 1 circular MOSFET device with W = 1 mm
- ➔ 2 circular diodes on the epilayer and the P-well region, respectively
- ➔ 2 MOS capacitors on the epilayer and the P-well region, with an area of 400 × 400 μm^2
- ➔ 2 combined TLM-Kelvin structures on the substrate and the P-well region
- ➔ 1 TLM structure; 1 Hall structure; 1 VDMOS device

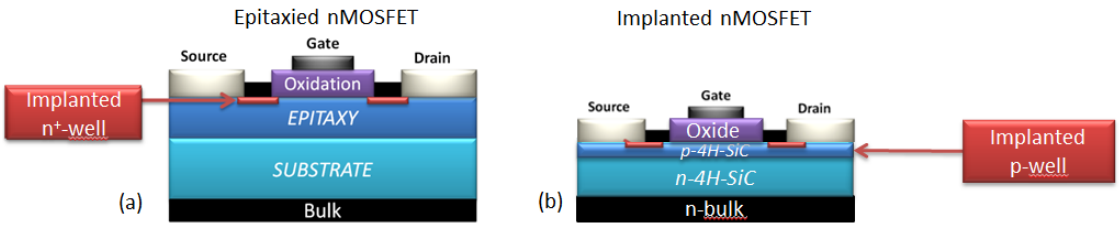

Fig.1.12. ***Schematic cross-section of a Lateral MOSFET structure including the key technological steps. A lateral MOSFET can be epitaxied (a) or implanted (b).***

In the manufacture process flow of a lateral MOSFET, the key stages follow this order: substrate growth, epitaxy deposition, doping and oxidation. One of the main efforts has been dedicated to the oxidation process, because it is one of the most complex steps in the component manufacture. Indeed a good oxide quality induces good channel mobility with a low threshold voltage and a high breakdown voltage, leading the component to accomplish its utmost performances. Two types of nMOSFETs can be fabricated: Epitaxied MOSFETs [Fig.1.12.a] and implanted MOSFETs [Fig.1.12.b].

1.3. Conclusion on the SiC MOSFETs challenges

In the semiconductor field, SiC is a wide band-gap (WBG) material that is taking a growing place due to its superior electrical and thermal properties over Si. Together with the recent improvements in the SiC crystal growth, SiC structures are currently offering a viable solution for replacing Si devices for harsh environment application. Among the current studied WBG materials, such as GaN or Diamond, SiC has the unique potential to be thermally oxidized to form a SiO_2 film. In comparison with the main SiC polytypes, 4H-SiC is the one whose bulk resistance presents the lowest values and where the isotropy of mobility versus crystal orientation is the most uniform, making it the most suitable concurrent semiconductor for vertical high power MOSFETs. However, so far, these devices have not reached the expected high performance and reliability. The 4H-SiC MOSFET still suffer from a low oxide quality, with a high amount of interface state density. These defects are responsible for the devices low field effect mobility, being one of the main drawbacks of the current fabricated SiC MOSFET devices. Therefore, the current challenges consist into extending the device fabrication, hence improving the gate oxide quality and reliability.

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Chapter 2

Electrical Characterization Methods

This chapter describes all the electrical measurements performed in order to complete full electrical characterization of MOS capacitors and transistors. Calculation methods for evaluating the main electrical parameters are also detailed. The most adopted method to extract the interface state density is also discussed. Finally, time bias stress and temperature measurements are introduced.

2.1 Capacitance Measurement by Mercury Drop Electrode Technique

In order to avoid any metal deposition, the MOS structure is only made by oxidizing the epitaxied wafer. Then, one can proceed with the electrical measurements using a mercury electrode probe station [1]. This is an accurate tool that enables fast, convenient, and non-destructive measurements of samples by probing wafers with mercury to form contacts on well-defined areas. This contact also allows various thermal or chemical oxide treatments without the limitations imposed by metallic electrodes on the oxide. Such an electrode is made by dropping mercury with a capillary under vacuum; sometimes involves vacuum problems and capillary diameter limitations. It is however one of the most suitable tool for SiO_2/SiC interface measurements. The main objective of C(V) measurement is to determine the oxide thickness and effective charge density (N_{eff}), and to have an estimation on the SiO_2/SiC interface fixed charge density (N_{fc}) obtained from the flatband voltage (V_{fb}) shift (section 1.2.3). The closer the V_{fb} to the theoretical flatband voltage (V_{fbth}) and the lower N_{eff}, the better the interface quality. N_{eff} is given by:

$$N_{eff} = \frac{Q_{eff}}{q \times A_{metal\_contact}} \quad (2.1)$$

where q is the electron charge in coulombs, $A_{metal\_contact}$ the metal contact area in cm^2 and Q_{eff} the effective oxide charge. This last parameter can be deduced from (2.2):

$$Q_{eff} = -(V_{fb} - V_{fbth}) \times C_{OX} \quad (2.2) \quad \text{with} \quad V_{fbth} = W_m - \left(W_s + \frac{E_g}{2} + \phi_b\right) \quad (2.3)$$

where C_{ox} is the oxide capacitance (the maximum capacitance value in the accumulation regime at low frequency), V_{fb} is the measured flatband voltage, V_{fbth} is the theoretical flatband voltage, W_m is the metal work function, W_s the SiC work function, Φ_b the bulk potential and E_g the bandgap energy. In an n-type MOS capacitor, majority carriers are electrons. Thus, the substrate potential is expressed by equation (2.4) and by equation (2.5) for a MOS p-type capacitor:

$$\phi_b = \frac{kT \ln(\frac{N_{bulk}}{n_i})}{q} \quad (2.4) \quad ; \quad \phi_b = -\frac{kT \ln(\frac{N_{bulk}}{n_i})}{q} \quad (2.5)$$

On the other hand, N_{fc} is determined by equation (2.6):

$$N_{fc} = \frac{C_{OX} \times |\Delta V_{FB\_HRTH} - \Delta V_{FB\_IL}|}{q} \quad (2.6)$$

where ΔV_{FB_HRTH} is the flatband voltage difference between the return hysteresis of the experimental MOS structure and the theoretical flatband voltage, and ΔV_{FB_IL} is the interface ledge hysteresis (see fig. 2.6).

The software used to treat the C-V data is a version of ICS, a powerful instrumentation control and data analysis package thought to control semiconductor test equipment used for device characterization. In the framework of this dissertation, C-V measurements were carried out on MOS structures mainly using the high-low frequency capacitance method [1]. The quasi static (low frequency) measurements allow determining the flatband voltage, the oxide capacitance, the flatband voltage hysteresis and the amount of fixed and effective oxide charges. The high frequency (1MHz) measurements provide an estimation of the interface state density (D_{it}) profile either below the conduction band or above the valence band, depending on the doping type of the semiconductor. This method only gives a D_{it} estimation since the calculation is made on a MOS capacitor instead of the nMOSFET area. However, this method accurately estimates the oxide quality prior to MOSFETs fabrication. Consequently, if all the mentioned electrical parameters measured on MOS capacitors show acceptable results (V_{fb} close to its theoretical value, $0V<\Delta V_{fb}<1V$, $N_{eff}<10^{12}$ cm^{-2}, $D_{it}<10^{12}$ $cm^{-2}.eV$), then MOSFETs fabrication with the appropriate oxide quality can start.

2.2. Transfer Length Method

By definition, the transfer length method (TLM) represents a metal/semiconductor (M/Sc) contact with a very low ohmic contact resistance (R_c). It is called “ohmic” because its electrical characteristics are in accordance with the Ohm’s law $R_c=V/I$, where V is the applied

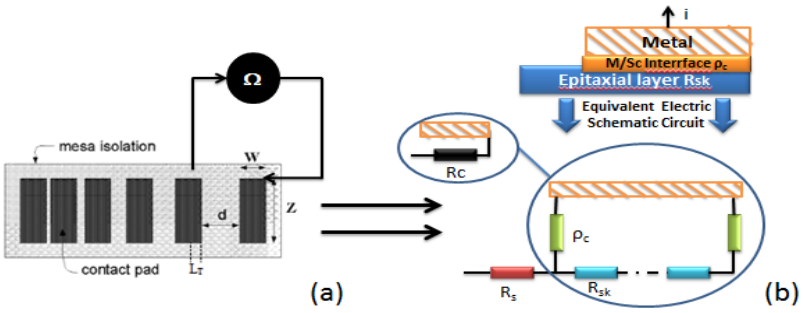

Fig.2.1: Measurement method of TLM. The resistance is measured by placing a tip probe between two pads (a) d is the distance between two pads, Z is the pad length, W the width and L_T the transfer length which is the average distance that an electron travels in the semiconductor beneath the contact before it flows up into the contact. The equivalent electric schematic is shown (b).

voltage and I the current crossing the M/Sc system [Fig.2.1.a]. The contact resistivity (ρ_c) is a parameter deduced from R_c (eq (2.7)), and it is expressed in $\Omega.cm^{-2}$ [2-4]. The typical range of ρ_c in n-type 4H-SiC and 6H-SiC varies from 10^{-4} $\Omega.cm^{-2}$ to 10^{-6} $\Omega.cm^{-2}$, which is higher that measured on lower bandgap semiconductors. The TLM method is the most common experimental procedure to determine the contact resistance.

In order to ensure a good uniformity of the MOSFET fabrication process, this value must be uniform across the wafer. The contact resistivity measurement requires the use of several isolated resistance patterns with different spacing integrated on the same chip as the MOSFET [5]. In SiC technologies, the ohmic contact is usually made by sputtered nickel followed by a 950ºC anneal for 180s. The metal resistance is assumed to be neglectible because of its high conductivity. R_{sk} is the semiconductor contribution just under the metal layer which is different from the semiconductor resistance (R_s) since the thermal annealing produces the metal alloy formation during metallisation process. The contact resistance (R_c) represents the contribution of the thin zone at the M/Sc interface to the total resistance of a TLM pattern. The calculation of the specific contact resistance by the TLM method is based on the Berger model [5]:

$$R_C = \frac{\sqrt[2]{\rho_C \times R_S}}{Z} \qquad (2.7)$$

The ρ_c extraction is carried out in three steps:

è **Step 1:** R_T, is the resistance measured on a TLM pattern, which is extracted from the IV measurements for different distances between two pads [Fig.2.2.a].

è **Step 2:** R_s and R_c are evaluated from the experimental $\Delta R_T/\Delta d$ values. R_s is determined by the experimental slope while Rc is given by the R_T extrapolation value for d=0 [Fig.2.2.b].

è **Step 3:** The contact resistivity is evaluated from eq.(2.7).

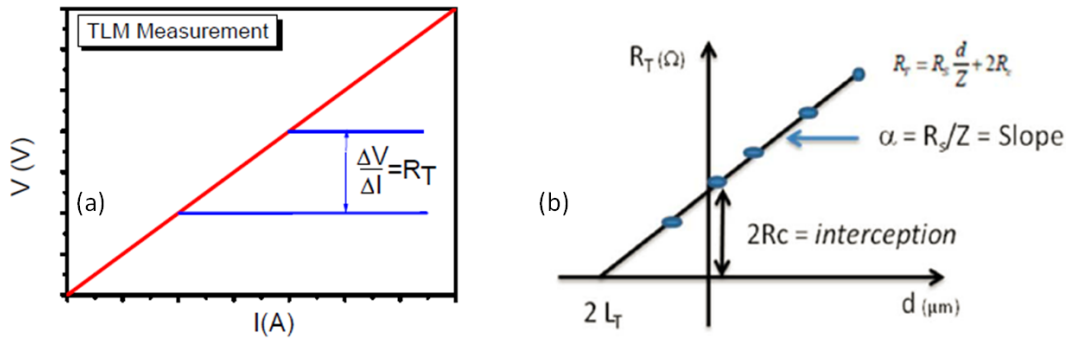

Fig.2.2. Total contact resistance extraction from I-V curves (a) and Total contact resistance versus distance, allowing contact resistivity calculation (b).

In general, the contact resistance is negligible in comparison with the on-channel MOSFET resistance, and does not have an important contribution in 4H-SiC MOSFETs with channel lengths larger than 8 μm. However, its contribution becomes more significant for lower channel lengths, contributing to drastically decrease the experimental field effect mobility (μ_{fe}) as it will be shown later [Fig.2.4.a]. Thus, a high contact quality is required to prevent the μ_{fe} decrease with the channel length.

2.3. Field effect mobility and threshold voltage extraction method

The extraction of all electrical parameters is mainly carried out from the I_{DS} (V_{GS}) and I_{DS} (V_{DS}) curves, using the Keithleys IV 24XX series system. The gate leakage compliance is fixed at 1 μA; at this current the measurement automatically stops. The threshold voltage is extracted from the I_{DS} (V_{GS}) curve by using the current constant method [6] with a predetermined drain current value. Although there is a lack of agreement about this current value, we have chosen it as 10 nA since it has been the most widely used in our laboratory in previous works. This method seems to be the most adopted one for devices' measurement because it allowed avoiding plenty of issues related with the noise caused by the second derivative of I_{DS} (V_{GS}) curves [7]. The field effect mobility (μ_{fe}) is extracted from the transconductance at a low drain voltage (V_{DS}=0.1V), and calculated according to equations (2.8, 2.9 and 2.10):

$$\mu_{fe} = g_m \times \frac{L}{W \times C_{OX} \times (V_{DS})} \quad (2.8) \qquad \text{with } g_m = \frac{\partial I_{ds}}{\partial V_{GS}} \quad (2.9) \quad \text{and} \quad C_{ox} = \frac{\varepsilon_{OX}}{T_{OX}} \quad (2.10)$$

where L is the channel length, W the channel width, g_m the transconductance, C_{ox} the gate oxide capacitance per unit area, T_{ox} the gate oxide thickness and ε_{ox} the silicon dioxide permittivity.

All the devices are tested at wafer level using a standard probe station. The output characteristics I_{DS} (V_{DS}) are obtained by applying positive voltages to the drain and gate while keeping the source grounded, as described in Chapter 1. These output characteristics can also be used for determining the field effect mobility (see section 3.3.3). The I_{DS} (V_{GS}) transfer characteristics are generally measured by applying a constant drain bias equal to 100 mV (MOSFET linear regime). The gate-drain leakage is firstly measured and, in general, has to be around 100 pA. The interface state density can also be obtained from the I_{DS} (V_{GS}) characteristics, the extraction technique being detailed in the following paragraph. Once the parameters' extraction is done, more complex measurements can be performed to monitor the threshold voltage stability at different time and temperature bias stresses.

2.4. D_{it} extraction techniques

2.4.1 A short description of the charge pumping technique and its issues

In the last decades, charge pumping (CP) current techniques have arisen as a powerful characterization tool to assess the semiconductor/dielectric interface in Si MOSFETs [8]. Contrarily to indirect C-V techniques used in MOS capacitors, CP allows determining the interface state density (D_{it}) directly on small geometry MOS transistors. Moreover, it is an easier technique compared with other methods like the conductance or deep level transient spectroscopy (DLTS), and it also provides more accurate results than those obtained from qualitative indirect techniques based on weak inversion conduction or 1/f noise [8]. In the last

years, the CP technique has been successfully applied, for example, to the characterization of deep-submicrometer MOSFETs and to the analysis of degradation induced by electrical stress or radiation-induced damage [9-10]. More recently, some studies have been carried out with this technique to characterize SiC MOSFETs. In particular, the scannable energy amplitude with CP method is a function of the pulse rise and fall times [11] and, in the used experimental conditions, the assessed energy range was about 2.5 eV in the middle of the 4H-SiC band-gap [12]. However, in 2015 *A.Salinaro et al.* successfully succeeded in characterizing the quality of the SiC/SiO_2 interface near the conduction and valence band edges, and pointed out the fact that both the transistor geometry and structure have to be carefully chosen [13]. Unfortunately, the mask set designed for MOSFETs fabrication does not allow the inclusion of the required geometry type for an accurate CP characterization, this fact explaining the abnormal high D_{it} values we previously obtained from CP measurements on MOSFETs [14]. Therefore, D_{it} electrical characterization on fabricated MOSFETs has to be performed otherwise. In this sense, another powerful tool for D_{it} electrical characterization is the subthreshold slope technique in the weak inversion region [15-16]. This extraction technique requires the surface potential ϕ_s for determining the scannable energy D_{it} amplitude.

2.4.2 Subthreshold slope method in weak inversion

If a classical interface between two heterostructures is considered, the periodicity of the crystal material changes from one material to another. Thus, different electronic states from the jointed material are created at the interface, called interface states. In a MOS structure, the applied voltage drops across the oxide and the semiconductor surface, inducing conduction and valence bands bending. This band-bending evidences the existence of a potential difference between the semiconductor surface and its bulk. The surface potential represents the barrier height (band-bending) that one carrier coming from the semiconductor bulk has to overcome in order to reach the surface [17-18]. In the MOS structure operation, the interface states playing an important role are those introducing allowed energy levels within the bandgap, because they can trap free carriers as the constant Fermi level crosses the interface states' energy levels in the bandgap, thus changing the surface free carrier concentration in the conduction and valence bands. The surface potential is given by (eq. 2.11):

$$\phi_s = -(E_{cs} - E_{cb})/q \tag{2.11}$$

where E_{cs} and E_{cb} are the semiconductor energy levels at the surface and at the bulk, respectively. In weak inversion, the surface potential can be modeled fairly accurately by considering the capacitive divider between C_{OX} and the semiconductor depletion capacitance C_{DEP} (considering the semiconductor bulk bias equal to zero) by using the following equation:

$$\phi_s = \frac{C_{OX}}{C_{OX} + C_{DEP}} \times V_{GS} \tag{2.12}$$

C_{DEP} is the depletion capacitance and its value is obtained by subtracting the accumulation capacitance from the capacitance obtained in the depletion region [19]. In this way, it is determined a direct relation between the surface potential and the gate voltage, which can be use to extract the D_{it} profile within the bandgap. In the weak inversion region of an n-channel MOSFET, the slope of log(I_{DS}) versus V_{GATE} curve is affected by the capture of free electrons by the interface states. The subthreshold slope $S = \frac{\partial V_{GATE}}{\partial log I_{DS}}$ is correlated to the density of the interface states by [20]:

$$S = \frac{k \times T}{q} \times (1 + \frac{C_{DEP} + C_{it}}{C_{OX}}) \times \ln(10) \quad (2.14)$$

where $C_{it} = q \times D_{it}$ and $C_{DEP} = C_{ox} - C_{\min\_dep}$. $C_{\min\_dep}$ is the capacitance in the deep depletion region. From these introduced equations, D_{it} can be deduced (2.15) as:

$$D_{it} = \frac{\left(\frac{\partial V_{GATE}}{\partial log I_{DS}} \times \frac{q}{k \times T} \times \frac{1}{\ln(10)} - 2\right) \times C_{ox} + C_{\min\_dep}}{q} \quad (2.15)$$

Thus, the D_{it} profile can be directly extracted from the MOSFET transconductance characteristics, and can be plotted as a function of the trap position above the valence band.

2.5. Bias Temperature Instability (BTI)

CNM offers the possibility to perform high temperature measurements up to 300°C thanks to a TC 200 TEMPCHUCK controller from Wentworth Laboratories, including a CAL 9500P temperature regulator connected to the chuck of a probing platform Pegasus S200 from Wentworth Laboratories. The main objective of such a measurement is to know the thermal behaviour of the main electrical parameters and, especially, that of the field effect mobility and the threshold voltage. Contrarily to Si material, the field effect mobility in SiC increases with temperature. Concerning Si-MOSFETs, the phonon scattering phenomenon (lattice vibration) together with the impurity scattering are at stake. At low temperature values (well below room temperature), the field effect mobility tends to increase when rising temperature since impurity-scattering predominates. A further temperature increase tends to decrease the mobility because the phonon scattering prevails [21]. However, a third phenomenon has to be taken into account in SiC, which is related to the SiO_2/SiC interface charges scattering. Due to the high amount of D_{it}, this scattering mechanism predominates in SiC, and it is more remarkable than in Si. At low temperatures, the field effect mobility is very low due to the presence of the charge trap and interface states that can either collide with the electrons and/or trap them. With the increase of temperature, electrons move faster and, therefore, the collision probability between electrons and the interface charges is consequently reduced, accounting for the increase of the field effect mobility even at room temperature [Fig.2.4.a]. However, for very high temperature values (>300 ºC), scattering with lattice vibration starts to predominate over the other scattering

mechanisms, and consequently, the field effect mobility starts to decrease. The temperature value at which this behaviour is observed depends on the oxide quality; i.e., the most free of defects at the SiO_2/SiC interface the lowest temperature value at which phonon scattering predominates.

Moreover, few electrons induced by the positive gate voltage are trapped, and consequently, coulomb scattering centres are also produced [7][22]. K.Matocha and V.Tilak explained the experimental mobility behaviour observed in the SiC inversion layer of a lateral MOSFET using conventional nitride gate oxides [23-25]. Briefly summarized, the field mobility increases with the gate voltage and reach a maximum value, corresponding to the saturation point. Once this maximum is reached, the field effect mobility starts decreasing when increasing the gate voltage due to the roughness scattering.

Concerning the threshold voltage (V_{TH}) temperature dependence, it drastically decreases when rising temperature due to the temperature sensitivity of the bulk potential and the corresponding reduction of filled interface state density. An example of the threshold voltage evolution with temperature is shown in [Fig. 2.4.b] where the V_{TH} decrease can be clearly seen. The impact of the channel length on V_{TH} is also shown in the figure.

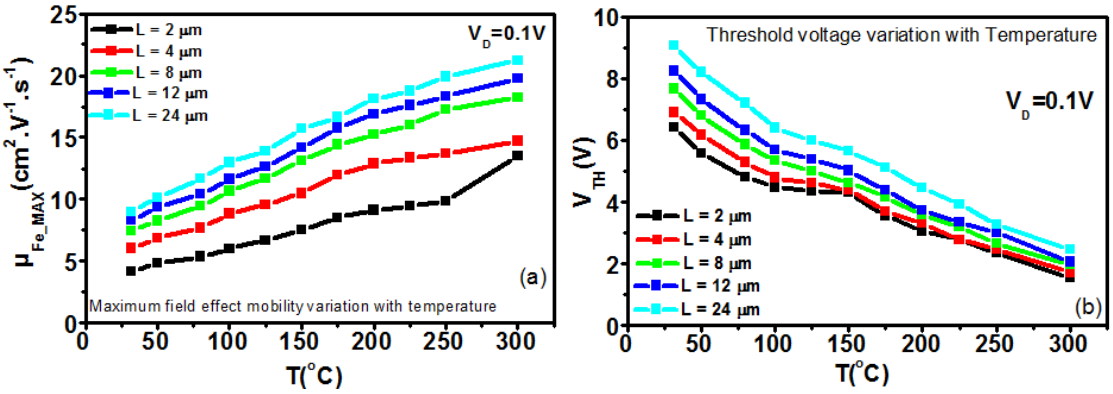

Fig.2.3. Threshold voltage (a) and field maximum field effect mobility (b) temperature and channel length dependence of a 4H-SiC nMOSFET. Under this measurement condition, the channel width W=150µm.

2.6. Time Bias Stress Instability (BSI)

The time bias stress instability (BSI) measurement is needed to evaluate the MOSFET electrical degradation with time by observing the impact of both the near-interface oxide traps and mobile charges on the device electrical parameters. Indeed, these interface traps, which are one of the main causes of MOSFET degradation with time, contribute to a large shift of the threshold voltage, to raise the reverse drain current and to increase the gate leakage current due to band-to-band tunnelling in the drain region underneath the gate [26-29]. In this way, BSI measurements are carried out with the time cycles described in [Fig.2.5.a] using the measurement equipment described in section 2.3 [30]. Initially, the gate voltage was generally ramped from -Vgate to +Vgate with a drain bias of 100 mV. Then, the positive gate bias is

maintained for different bias stress times (10s, 36s, 100s, 360s, 1000s and 3600s) while the other terminals remain grounded. Following this positive bias stress, the gate voltage was ramped from +Vgate to -Vgate to determine the shift of the $I_{DS}(V_{GS})$ characteristics. In general, three threshold voltages are extracted during the BSI measurement. The two first are the threshold voltages after a negative and a positive bias stress (V_{TH_NBSI} and V_{TH_PBSI}, respectively), while the third one is the threshold voltage hysteresis ΔV_{TH}, which is the threshold voltage difference between V_{TH_NBSI} and V_{TH_PBSI}. The plot of ΔV_{TH} versus bias stress time provides information on the hysteresis time stability and on its amplitude variation with time. The Vgate value is chosen to characterize only the instability due to native traps, avoiding the creation of new defects. Therefore, relatively low voltage stresses (E < 3 MV/cm) have been applied [31]. In few words, BSI is caused by two effects including mobile charges, accounting for an increase of the interface traps and electron trapping. It is usually characterized by monitoring the threshold voltage shift as shown in [32] by the following equation (2.16):

$$\Delta V_{TH} = \frac{q \times (N_{it}+N_{ox})}{C_{OX}} \tag{2.15}$$

The evolution of the MOSFET subthreshold current with bias-stress can also be used to detect near-interface oxide traps in the channel region. It also alters the drain leakage mechanism and results in an enhancement of the Gate Induced Drain leakage (GIDL) current [33] [see Fig.2.5.b].

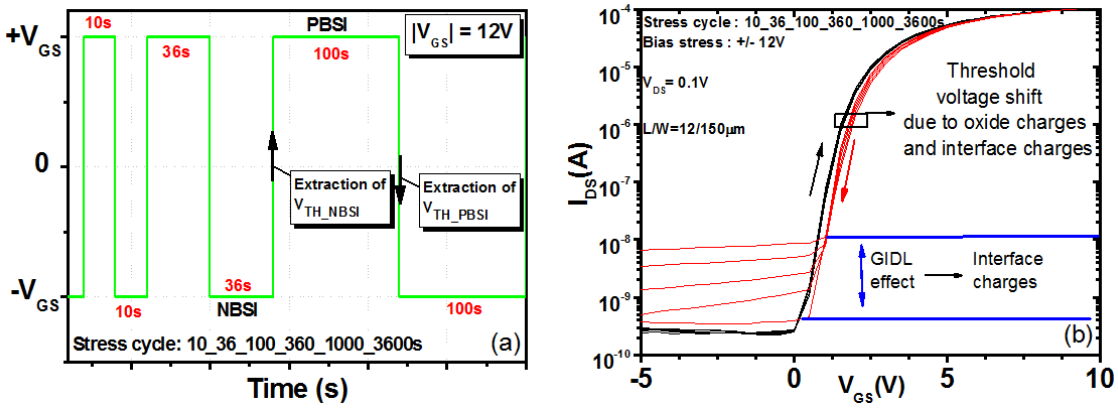

Fig.2.4. Schematic of bias-stress cycle showing the applied V_{GS} versus time during the gate bias-stress threshold instability measurements (a) and its correspondent $I_{DS}(V_{GS})$ curves showing the impact of interface charges and oxide charges on the I_{DS} GIDL and threshold voltage drift (b).

2.7. Conclusion on electrical characterization methods

Several electrical characterization techniques have been detailed, from the C(V) measurement to the classical $I_{DS}(V_{GS})$. In addition to the electrical characterization and to the gate oxide process, more complex measurement can be performed in order to monitor the V_{TH}/μ_{fe} time and temperature stability with bias stress. The most complex one is related with the D_{it} extraction above/below the valence/conduction band. In nMOSFETs, the D_{it} below the valence band can also be extracted. However, its value can be considered as second order if the field effect mobility is firstly extracted. Indeed, a very high value of the field effect mobility is the direct consequence of a low interface state density. In the MOS structure, D_{it} is one of the most important parameter, because its value together with the flatband voltage, the fixed charge and the effective oxide charge value directly inform about the oxide quality. However, a good MOS structure does not predict the fabrication of a high quality MOSFET, since the implantation well, the ohmic contact, the masking operation, the photolithography, the cleaning process, the p-epilayer/p-implanted process have to be very well controlled.

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Section 2

The Irradiation Parameter

Chapter 3
Proton Irradiation of 4H-SiC MOSFETs with Oxynitrided Gate Oxide

In this chapter, a complete study showing the impact of proton irradiation on 4H-SiC MOSFETs is presented. The charge build-up mechanism theory in Si-MOSFETs is given as a first approach. Then, the electrical parameters of irradiated MOSFETs in 4H-SiC having different gate oxides are presented. The different electrical behaviour from the one expected in the state-of-the-art of Si-MOSFETs imply to establish advance hypothesises based on the charge build-up that take into account the interface state.

3.1. Irradiation of Gate oxide MOSFETs in Si

3.1.1. Charge build-up and small polaron mechanism in SiO_2

The interaction of radiation with matter is a very complex issue. In long-term, degradation of MOS devices has to be avoided in different harsh irradiated environment, especially if the component is built for aerospace or military applications. Focusing the investigation on building an irradiated-resistive component containing a good interface quality is also one of the main objectives of this thesis. Thus, in a first time, it is important to have an idea about the irradiation impact of several types of particles on a Si- MOSFET, and more specifically, on its gate oxide. Up to now, irradiation on Si-MOSFET has been well understood [1], whereas very few studies on SiC MOSFETs have been carried out. The charged particles used in the frame of this thesis are mainly electrons (chapter 4) and protons. In the general theory [2], protons irradiation beam gives rise to the following phenomena:

1 → Coulomb interaction and collision with the nucleus which can cause two types of damages in the crystal lattice: Free carrier generation by the incident radiation beam, and atom displacement within the crystal lattice if the incoming proton energy is high enough and transferred to the nucleus. These events occur for all energies.
2 → Nuclear reaction which can occur for protons energies higher than 10 MeV.

The most important mechanism when irradiating a MOSFET gate oxide is the ionization which means that hole-electron (e-h) pairs are created. Indeed, when a particle penetrates in the oxide layer and the epilayer [Fig.3.1.a], various bonds between atoms can be broken, generating e-h pairs [Fig.3.1.b], and forming dangling bonds. Then, three different cases of the charge build-up mechanism can be distinguished:

Case nº1: Irradiation of an ideal oxide without gate bias

In the case of very few amount of oxide charges and SiO_2/Si interface traps, the e-h pairs generated by the transferred energy recombine instantaneously after being separated as shown in [Fig.1.c] and [Fig.1.d]. In this case [3], the irradiation does not affect the oxide quality and no damage is induced. However, if the irradiation energy is low enough for allowing the incident particle to stop inside the oxide, the particle would act either as an additional interface charge or as an impurity within the oxide.

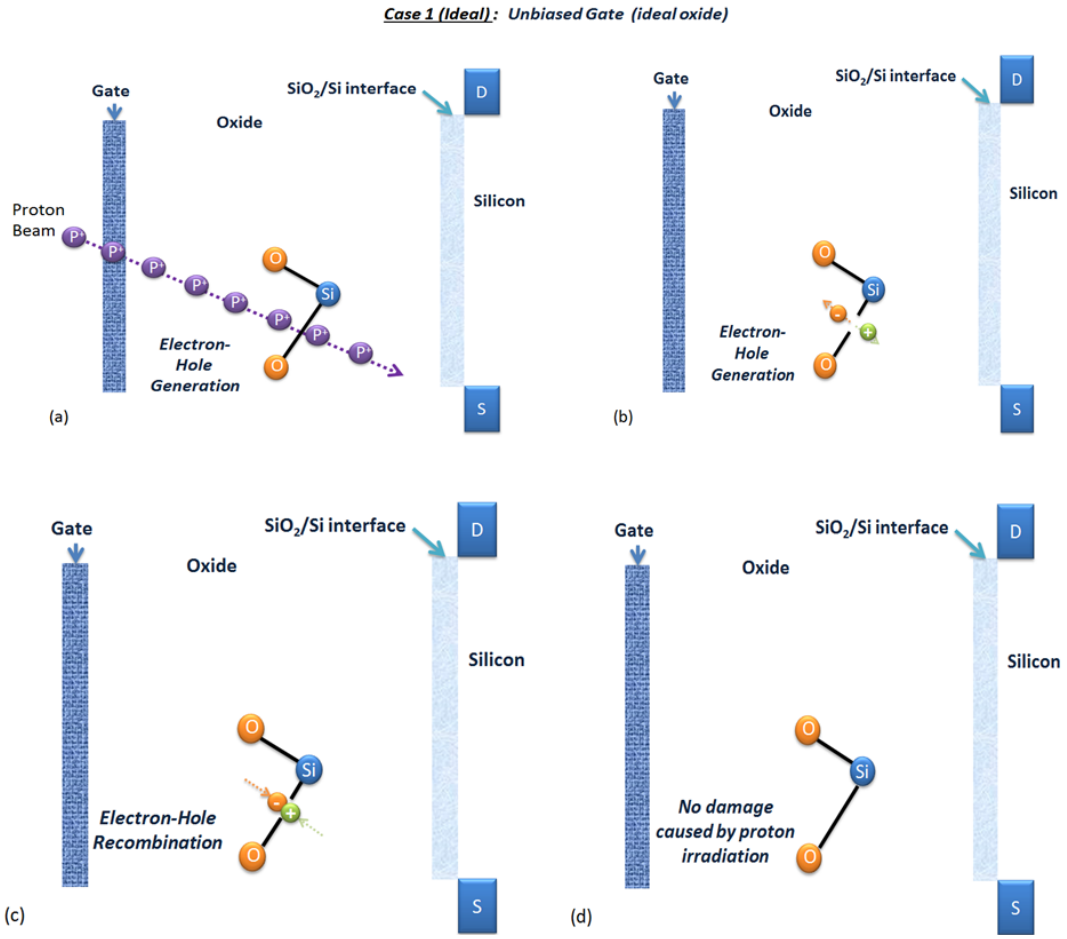


Fig.3.1. Step-by-step description of the charge build-up mechanism under unbiased conditions in a perfect oxide

Case nº2: Irradiation of an ideal oxide with a positive gate bias

As mentioned before, when the particle crosses the SiO_2 layer, it generates e-h pairs that can recombine in first picoseconds if the gate is unbiased. However, when a positive bias is applied to the gate, most of the electrons resulting from this generation swept out through the gate due to the existing electric field. This electric field sweeps out the generated holes in the opposite direction, but contrarily to the electrons' case, holes tend first to remain near it point of generation. As a result, hole motion toward the SiO_2/Si interface is a much slower process than

the electron displacement to the gate. Hole transport toward the interface will contribute to increase the amount of positive interface traps [3]. This hole transport phenomenon can last up to several seconds at room temperature and up to several hours at lower temperatures. The hole transportation theory is called the *small polaron mechanism* [4]. It is based on the strong interaction between the generated hole and the crystal lattice. Once generated, the hole carrier polarizes its surrounding environment and this polarization interact back to the carrier. If the interaction is sufficiently strong, with a large distortion of the lattice in the immediate vicinity of the carrier, the carrier becomes localized at a particular site. This self-trapped carrier is called "small polaron". When an initially empty localized trap site [Fig 3.2.a] captures a hole, the total potential is lowered by a distortion of the lattice around the trap site. The hole adds its potential to the initial one and is self-trapped [Fig 3.2.b]. When it moves through the oxide, it carries with it the potential well arising from the distortion of the lattice. The transition of the hole between two nearby sites occurs via the intermediate state [Fig 3.2.c] which is thermally activated by thermal fluctuation of the system. These momentarily bring the electronic energy level of the two sites into coincidence, so that the hole can tunnel from state (1) to state (2). The final state is shown in [Fig 3.2.d]. By moving according to the polaron hopping transport phenomenon, finally holes accumulate at the SiO_2/Si interface as acceptor traps. As a consequence, electrons in the Si substrate are more easily attracted by the trap and can tunnel toward the interface layer for trap neutralization.

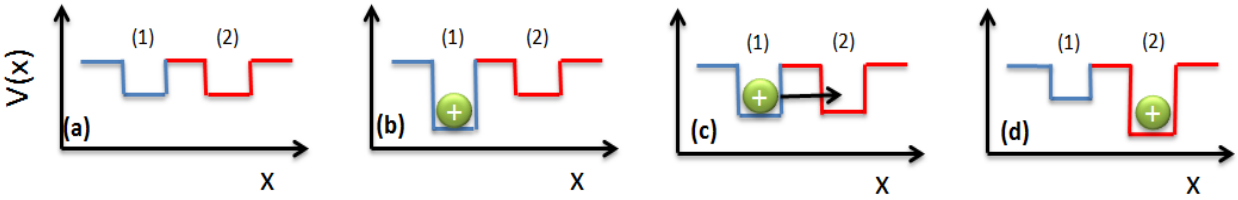


Fig 3.2. The polaron hopping transport phenomenon (adapted from [5])

Case nº3: Irradiation of a non-ideal oxide with or without gate bias

In this case, the oxide is considered as imperfect which means that interface traps, ion mobile charges, fixed charges and oxide trapped charges have to be taken into consideration. If the gate terminal is unbiased, e-h pairs generated by the irradiation particles crossing the gate oxide [Fig 3.3.a] cannot recombine due to the charge interaction between the generated charges and those existing within the dielectric [Fig 3.3.b]. The above mentioned original oxide charges may either trap or repel the generated e-h depending on their charge nature, thus do not allowing them to recombine [Fig 3.3.c]. In the case that a positive bias is applied to the gate after irradiation, the generated carriers' motion is the same as in Case nº 2 (see Figs 3.3.d, e and f). On the other hand, if a negative bias is firstly applied to the gate after irradiation, the generated electrons move toward the oxide interface while generated holes slowly move in the opposite direction to the gate. Electrons normally cannot sweep out from the oxide and may be trapped either in the oxide or the SiO_2/Si interface by falling into a charge trap. However,

electrons reaching the interface can also either tunnel into the epilayer or recombine with a hole tunnelling into the oxide.

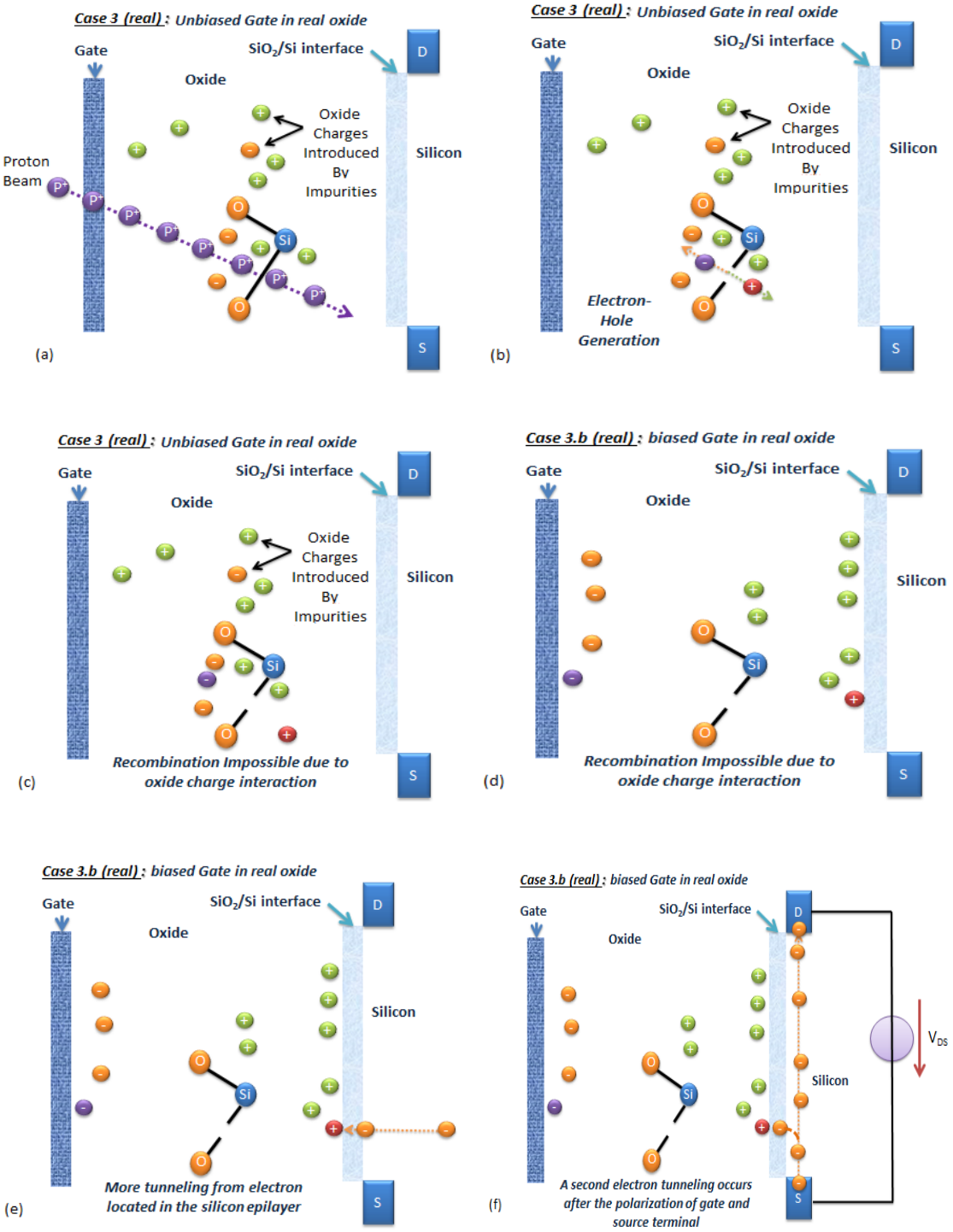


Fig.3.3. Charge build-up mechanism in a real oxide of Si MOSFET with biased gate voltage. The particle cross de device (a), generates e-h pairs (b) that do not recombine due to the charge interaction (c). The gate is positively biased afterward (d) and can induce tunnelling of electrons coming from the epilayer (e) or coming from the source-drain terminal if V_{DS} is applied (f)

3.1.2 Radiation effects in Si nMOSFETs

The charge build-up mechanism impact on Si-nMOSFET is generally very strong and in most of cases lead to [6-9]:

➔ Lowers the transconductance and field effect mobility. This decrease is related to the increase of the interface traps. The driving capability of the device is decreased.

➔ Drifts the threshold voltage (V_{TH}). Irradiation induces traps generation with energies within the Si bandgap. Experiments have shown [10-11] that most of the interface traps with energies above the midgap are acceptors whilst traps with energies below act as donors. Thus, for n- and p-channel MOSFETs, V_{TH} increases in absolute value after irradiation due to charge capture by the interface traps during the transistor conduction process. In an n-channel MOSFET, the acceptor traps below the Fermi level will trap electrons, thus becoming negatively charged. Therefore, a higher gate voltage will be needed to create the channel inversion. The same argument applies for a p-channel MOSFET, where donor traps in the lower part of the gap capture free holes. As a result, the V_{TH} shift is positive for an n-channel MOSFET and negative the p-channel counterpart.

➔ Radiation also results in a slow V_{TH} drift with time [12], and a distortion of I_{DS}-V_{GS} and C-V characteristics as a consequence of the polaron transport phenomenon. After irradiation [Fig 3.4.a], generated interface traps start to play a role later than the fixed charge within the oxide volume due to hole trapping [Fig 3.4.b]. Indeed, the interface states increase slowly compared to the build-up of oxide positive charges since it takes some time for the generated hole to move from its generation point to the SiO_2/Si interface. As a result, the V_{TH} shift of an n-channel MOSFETs can initially be negative before becoming positive, this phenomenon being known as "rebound" as explained by [13]. In the case of the V_{TH} shift remains negative, the number of negatively charged interface traps finally exceeds the number of trapped holes.

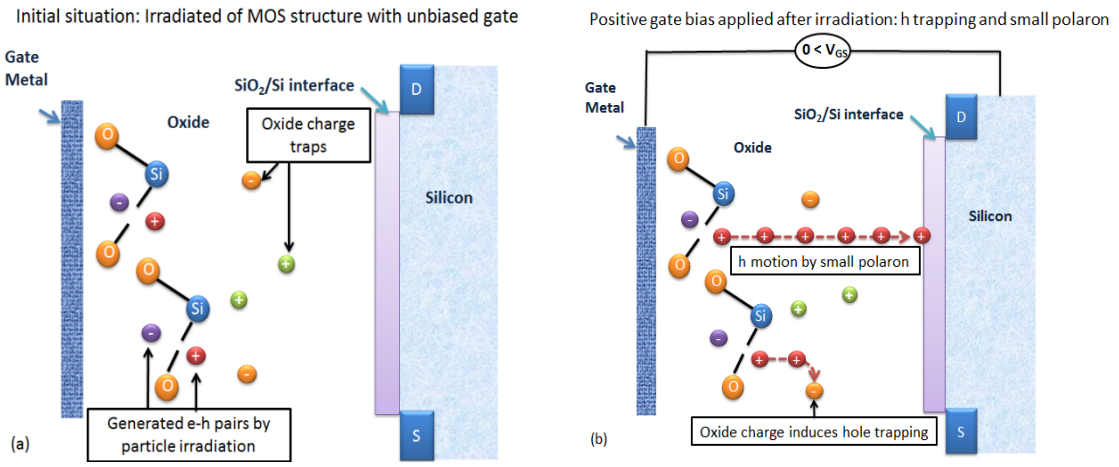


Fig 3.4 Charge build-up in a real oxide of Si-MOSFET irradiated with unbiased gate voltage (a). A negative gate voltage is applied to illustrate the hole charge trapping (b).

➔ Holes generated within the gate oxide favour electron tunneling from the Si layer, resulting in an increase of the gate leakage current. In addition, the oxide energy bands are more easily bended; resulting in an oxide breakdown for a lower gate voltage value than if the device was not irradiated.

The above mentioned effects account for the irradiation impact on both oxide and SiO_2/Si interface. On the other hand, the radiation effects on the semiconductor material can be categorized into 4 groups:

➔ *Impurity Production*, from the creation of hydrogen when a proton becomes neutralized either in the semiconductor bulk or in the p-epilayer/p-implanted layer.
➔ *Atom Displacement* from their normal position in the structure of the material. Displacement atoms may leave lattice vacancies and remain in interstitial locations, or cause interchange of dissimilar atoms in the lattice structure.
➔ *e-h pairs generation* in the path of the charged particles.
➔ *Large Energy Release* in a small volume, which can result in thermal heating of the material.

Although it seems that the most important effects on the MOSFETs electrical properties is due to the charge build-up mechanism in the oxide layer, there is also an impact of irradiation in the silicon bulk. Specifically, high energy particle beam may also provokes few bond-breaking inside the Si-substrate, generating e-h pairs that will contributes to creates vacancies, and will modify its doping concentration [14]. This effect is less remarkable although it must be taken into account in order to discuss about the results obtained in irradiated 4H-SiC MOSFETs.

3.2 Background of annealing impact on the electrical parameters recovery

Oxide trapped holes generated by irradiation are relatively stable, and their recombination process can extend for hours or even years, with a complex dependence on time, temperature, and applied field. The main idea of performing post-irradiation annealing is to facilitate the e-h recombination generated in the oxide in order to obtain a total recovery of the EPs in the best case. When the annealing process is performed, the gate can be either bias or unbiased. An irradiated sample has been annealed in [15] under a positive bias at 100ºC for about one week, and it has shown that all the trapped positive charges generated by irradiation were removed. But then, they applied a negative gate bias, and about half the neutralized positive charges were restored within a day. This suggested that annealing of radiation damage involved a compensation process: The defects were neutralized without being removed. Under a negative gate bias, a significant amount of neutralized positive charge reappeared, but there was also a significant amount of “true annealing” from which the trapped charge was really removed. Lelis et al. proposed a model illustrated in Fig 3.5 to account for their results [16] and those from other groups [17-22]. Generally, it has been assumed in the case of an irradiated

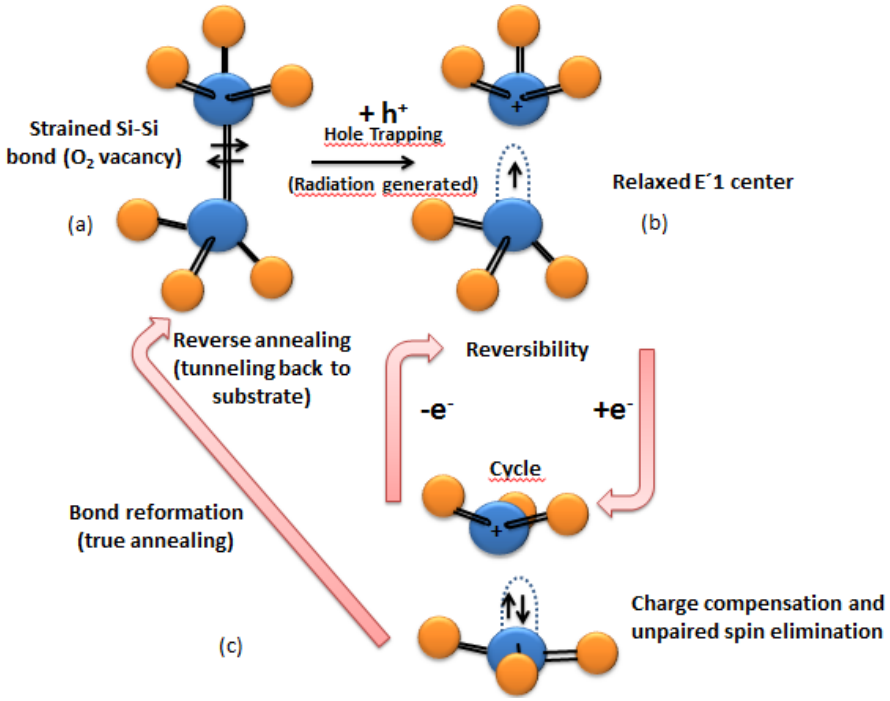


Fig.3.5. Recovery mechanism according to the state-of-the-art (adapted from [17]). The radiation induce hole creation (a) that that be trapped or can generate E' center (b). The annealing allows the bond reformation and provokes a charge compensation that will reform the original atomic structure (c)

Si-MOSFET, that annealing allowed an electron tunneling to the positively charged Si, neutralizing it, and re-establishing the Si-Si bond. Instead, Lelis proposed the electron tunnel to the neutral Si, forming a dipole structure, where the extra electron can then tunnel back and forth to the substrate in response to bias changes. In the transition from [Fig.3.5.a] to [Fig.3.5.b], the hole and its lattice distortion reaches a strained bond and tends to strain it further, leading in most of the cases to bond breaking and a trapping event. In Fig.3.5.b, the hole is trapped on one of the Si atom. Thus, Si atom is positively charged. The other Si remains neutral, with a dangling orbital containing one unpaired electron. These two trivalent Si atoms together constitute an E' center identified by Feig et al [23-24]. They believed that the simplest model which accounts for these observation [18, 25] is that the electron tunnels to the neutral Si where it joins the unpaired dangling electron, forming a spin pair (one spin up and one spin down), and leaving the Si negatively charged. Then, depending on the lattice relaxation, the broken bond may or may not re-establish. If a negative bias is applied before the broken bond reforms, the extra electron can tunnel back to the Si substrate, leaving a net positive charge in the oxide again. A second possibility is that the compensating electron tunnel from the Si conduction band to positively charged Si atom (an excited state), and then decays to the neutral Si atom [16]. The transition from [Fig.3.5.b] to [Fig.3.5.c] describes the switching and was reported by Lelis et al. [26]. Their group explained that if the trapped hole is only compensated by this trapped electron, then the process of "reverse annealing" can be readily understood, simply requiring that one of the two electrons on the now negatively charged Si atom tunnel back to the

substrate (returning to the configuration of [Fig 3.5.b]. The observation that some traps can be alternately filled and emptied is depicted by the arrows going both ways between [Fig 3.5.b] and [Fig 3.5.c]. The bond between the Si atoms can also be reformed, reflecting true annealing of the defect instead of compensation (long arrow back to Fig 3.5.a). If the gate is not biased during the annealing, the recombination process only depends on the time and temperature. In addition, the increase of temperature at V_{GS}=0V may induce a similar recovery effect described by a positive gate bias at room temperature. The hole discharge of hole trap commonly observed at or near room temperature is the major contributor to the so-called long term annealing of radiation damage in MOS devices. The annealing of the trapped holes has two manifestations that may reflect different hole-removal processes. The first is the slow bias-dependent recovery of the oxide charge traps, typically observed at normal operating temperatures (-55ºC to 125ºC) [27]. The second is the relatively rapid and strongly temperature-dependent removal or recombination of the holes observed when MOS structures are deliberately subjected to thermal annealing cycles at elevated temperatures (from 150º to 300ºC). This mechanism has been described through a thermal detrapping model [28]. Typically, the annealing effect on irradiated Si-MOSFETs it supposed to produce a partial or integral recovery of the electrical parameters induced by a recombination of the electron-hole pair generated by the irradiation near the SiO_2/Si interface, depending on the annealing time and temperature. In our case, the SiO_2 layer is grown by an RTP N_2O oxinitridation, and different behaviours have been observed. In the state-of-the-art, post irradiation annealed 4H-SiC of oxinitrided MOSFETs irradiated under proton beam has not been founded. The closer approach that was presented in is a description of irradiation annealed (PIA) effect of a 4H-SiC MOS capacitor having a nitride gate oxide, and irradiated with x-ray [29]. However, in these studies, the authors lead to conclude about an enhancement of the midgap voltage shift with the increase of annealing temperature due to the detrapping or compensating electron from N- and O- vacancy related in the near-interfacial SiO_2. However, in this study both, annealing and irradiation have been performed by applying a certain gate bias. In the frame of this thesis, neither irradiation nor annealing have been performed under gate bias condition, not only due to the issues related with carbon tape, but also, to limit the number of physical parameters that have to be taken into account during the PIA of 4H-SiC MOSFETs. V_{TH} stability and μ_{fe} variation might depend on many physical parameters such as e-h pair generation, N-diffusion, oxide and interface charge traps variation, e-h trapping-detrapping, hole transport, hydrogen impurity conversion in the epilayer for low irradiation energies, gate oxide thickness and on the different transition layers. By adding the gate bias parameter during the PIA, it may be complex to establish any conclusion.

3.3 Irradiation in SiC-MOSFET: A lack of information

After explaining the irradiation mechanisms in Si-MOSFETs, it is now relevant to make the transition to SiC MOSFETs. In the state of the art, irradiation in 4H-SiC MOSFETs under both electron and proton irradiation beams show the following effects: Al doping decrease [30],

creation of deep level defects [31-32], and carrier lifetime modification [33]. However, no electrical characterization of proton/electron irradiated 4H-SiC n-channel MOSFETs has been reported so far. Indeed, all the electrical characterization studies have been carried on 6H-SiC MOSFETs [34-36], on 4H-SiC JFETs [37], and on gamma irradiated 4H-SiC MOSFETs [38].

3.3.1 Understanding of the MOSFET threshold voltage shift

To explain the behavior of the electrical parameters that will be shown in this chapter (increase of μ_{fe}, no gate leakage current, time stability improved with BSI stress, etc…), it is necessary to foreseen what can occur when an oxynitrided dielectric layer is irradiated. In the state of the art, there was no reference about the peculiar electrical behavior of oxynitrided gate oxide in 4H-SiC under proton or electron irradiation. Thus, the following postulate is suggested.

We are in the case where the gate is not biased during the irradiation process. When the proton beam penetrates through the oxide, SiO_2/SiC interface and epilayer [Fig.3.6.a], e-h pairs are generated and various types of bonds between atoms get broken. In the oxide bulk, the bond between oxygen and silicon are mainly the one that get broken [Fig.3.6.b]. In the case of SiC MOSFETs, the charge density within the oxide is much higher than in Si. Thus, e-h pairs recombination cannot easily occur due to the oxide charge interaction (see 3.1.1 case Nº3). Moreover, an additional parameter interferes at the SiO_2/SiC interface, which is the high D_{it} amount that is present before the irradiation process. After the irradiation is performed, the MOSFETs is negatively biased. The generated electrons in the oxide move toward the SiO_2/SiC interface and can fall into an acceptor trap located either in the oxide bulk or in the SiO_2/SiC transition layer [Fig.3.6.c]. Additionally, hole tunneling from the SiC surface to the oxide can be trapped by donor traps at or near the SiO_2/SiC interface. [Fig.3.6.d]. When the gate bias switches from negative to positive, and the drain to source voltage is kept at 0.1V, holes located in the bulk oxide tend to slowly flow (polaron) toward the SiO_2/SiC interface while electrons tend to flow toward the gate metal. However due to the charge trapping, the amount of electron reaching the SiO_2/SiC interface during the negative bias is larger than those leaving the SiO_2/SiC interface after the bias starts to be positive, and the number of hole reaching the SiO_2/SiC interface during the negative bias is much lower than the generated one by charge build-up due to the small polaron transportation [Fig.3.6.e]. Thus, the V_{TH} drift does not depend only on the e-h generated in the oxide bulk but also, on those which may have been generated at the SiO_2/SiC interface and inside the epilayer (lattice damage). Independently of the gate bias, if at the SiO_2/SiC interface, the sum of generated donors accumulating at the interface predominates over the sum of acceptors at the interface, the MOSFET threshold voltage will be shift negatively. If the sum of acceptors is superior to the sum of donor at the interface, the threshold voltage will shift positively [Fig.3.6.f] with the V_{DS} bias. The experiment furtherly detailed revealed that generally, and with the increase of the dose, donors start to predominate at the SiO_2/SiC interface. But in some cases and with the increase of the dose, acceptors start being the predominating charges.

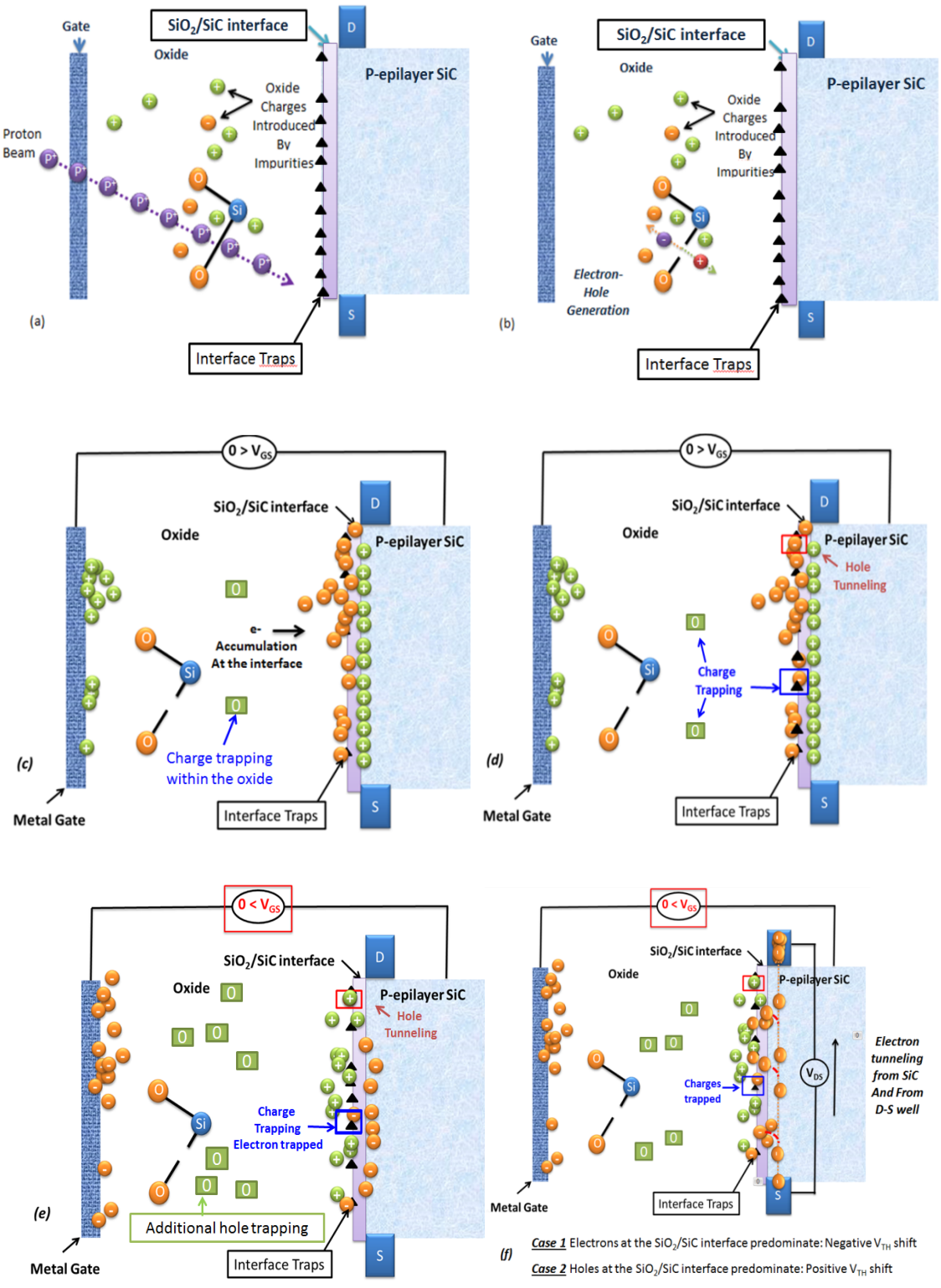


Fig.3.6. Charge build-up mechanism in a real oxide of SiC MOSFET with biased gate voltage. The particle cross de device (a), generates e-h pairs that do not recombine (b).The gate is negatively biased (c) and induce electron-hole accumulation at the SiO_2/SiC interface plus additional charge trapping at the SiO_2/SiC interface and at in the oxide bulk, and charge tunneling (d). Then, the gate is positively biased, electron and holes are switched (e). When V_{DS} is positive, the channel is created and can provoke electron tunneling (f).

3.3.2. Irradiation Set-Up of SiC MOSFETs and Gate Oxide process technologies

3.3.2.1. SRIM-TRIM simulation

SRIM (Stopping and Range of Ions in Matter) is a group of programs which calculate the stopping and range of ion beams into matter using a quantum mechanical treatment of ion-atom collisions. This calculation is made very efficiently by using statistical algorithms which allow the ion to make jumps between calculated collisions, and then averaging the collision results over the intervening gap. In the calculation process, the ion and atom have a screened Coulomb collision. A full description of the calculation method is found in the tutorial book [39-40].This book presents the physics of ion penetration into solids in a simple tutorial manner, and gives the source code for SRIM programs with a full explanation of the involved physics. TRIM (Transport of Ions in Matter) is the most comprehensive program included in SRIM. TRIM accept complex targets made of compound materials with up to eight layers of different materials. With this program, the proton beam penetration into SiC MOSFETs can be easily reproduced and simulated since only three layers are required (metal, oxide and SiC material). For the irradiation simulation, the key parameters are the type of structure, the number of layers, the selected atom for irradiation, the dose and the energy. The two more relevant results in the framework of this thesis are the proton beam penetration depth and its ionic distribution. However, the biggest drawback of SRIM simulator is the required time for a complete simulation

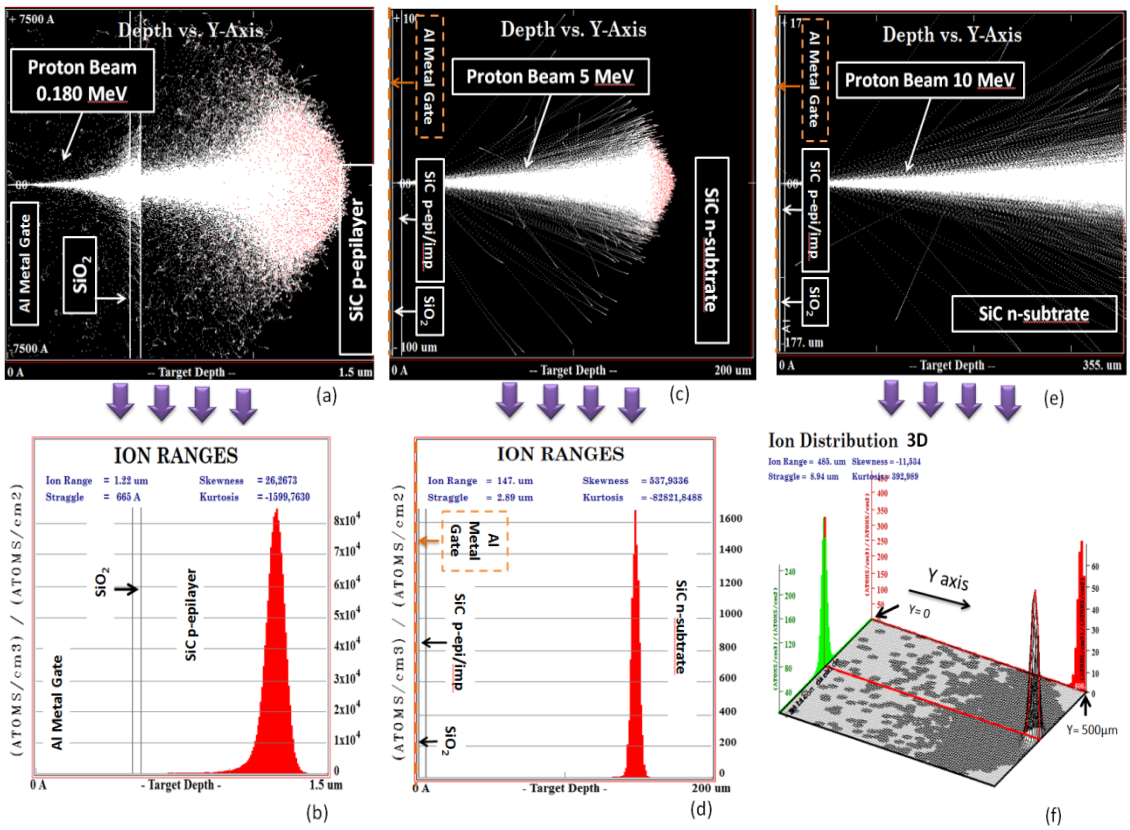


Fig.3.7. SRIM simulations and atomic distribution of a proton beam irradiated 4H-SiC MOSFETs at 3 energies: 0.18 MeV (a)(b), 5 MeV (c)(d) and 10 MeV (e)(f).

at high implantation fluence (for example, the simulation of a proton penetration within SiC material of an irradiation fluence of 5 x 10^{12} cm^{-2} takes more than 400 days). This is the reason why SRIM is mainly used for knowing how deep inside protons can penetrate and where they accumulate within the structure. Another SRIM limitation is the unavailability in simulating electron irradiation. As mentioned before, there are very few studies in the literature about the irradiation impact on 4H-SiC nMOSFETs having a standard gate oxide, but no information about electrical behaviour of irradiated oxynitridated gate oxide nMOSFETs has been reported. Then, an additional purpose of this work is to: establish preliminary hypothesis about electron and proton irradiation impact on 4H-SiC lateral nMOSFETs having an oxynitrided gate oxide. In the proposed experiments, the evaluation of proton and electron irradiations' impact has been carried out on p-type epilayer nMOSFETs. In addition, results of proton irradiation performed on p-type implanted layer are presented in chapter 6. For an accurate evaluation of the proton irradiation effect on nMOSFETs electrical parameters (EP), irradiation at three energies have been performed: 0.18 MeV, 5 MeV and 10 MeV, while electron irradiations were done at 15 MeV. At 0.18 MeV, the proton beam stops inside the epilayer [Fig 3.7.a], [Fig 3.7.b]. At 5 MeV, the proton beam stops inside the substrate [Fig 3.7.c], [Fig 3.7.d]. At 10 MeV, the beam completely crosses the nMOSFETs thickness (355 µm) [Fig 3.7.e], [Fig 3.7.f]. At this energy value, the proton beam will stop at 500 µm if the MOSFET substrate would be thick enough. Concerning electron irradiation at 15 MeV, the beam also crosses the MOSFETs substrate as in the third experiment. The fluences have been chosen in order to cover a wide range of applications. In terms of total doses, the proton fluence and the electron dose can be expressed according to: [41-42]:

$$D = \frac{F \times E}{R_p \times \rho} \tag{3.1}$$

where D is the dose in J/g, F is the fluence in number of particle/cm^2, E is the beam energy in eV, R_p is the penetration depth of the irradiation beam in cm, and ρ is the target semiconductor density. The dose and fluence unit in the international unit system (SI) is the joule per square metre (J/m^2), but, in most of the articles founded in the literature, radian (rad) seems to be the common unit [13, 43,44]. Given that 1 gray (1 Gy=100 Rad) is equal to 1 J/Kg, and that 1 MeV is equal to 1.602 x 10^{-13} J, the absorbed fluences and doses can be converted in Mrad, as shown in Table 3.1 below.

Particle type	Proton		
Energy (MeV)	0.18	5	10
Fluence (cm^{-2})	Mrad	Mrad	Mrad
5 × 10^{11}	3.68	0.87	0.51
5 × 10^{12}	36.81	8.75	5.14
5 × 10^{13}	368.1	87.50	51.45
5 × 10^{14}	Not irradiated	875.00	514.50

Table 3.1 Summary of the proton irradiation parameters used in the experiment: energy and fluence performed on the two different batches of SiC-MOSFETs (N_2O RTP and N_2O RTP + TEOS gate oxide).

3.3.2.2 Gate oxide process

The tested 4H-SiC nMOSFETs presented in this chapter include two types of gate oxides. Both MOSFETs types were processed on a 10 μm thick p-type epitaxial layers grown on Si-face 8ºoff-axis of 3 inch n-type 4H-SiC substrates. The epilayers have an Al doping concentration of 5×10^{16} cm^{-3}.

MOSFET#1: In the oxidation process of the first set of n-MOSFETs, the wafer was treated with HF and a conventional RCA cleaning prior to oxidation. After cleaning, the wafer was loaded at room temperature in a RTP furnace and a surface pre-treatment consisting of an in-situ RTA step in H_2 at 900ºC. Subsequently, the gate oxide was formed by rapid thermal oxidation (RTO) in 100% N_2O at 1050°C for 10 min, resulting in an average oxide thickness of 38 nm. The oxidation was followed by a 3 min annealing under Ar with a temperature ramp down from 1050ºC to 22ºC (clean room temperature). The oxidation process is presented in [Fig.3.8.a], and more information about this type of oxidation is given in section 1.2.4

MOSFET#2: For the second type of n-MOSFETs the cleaning has been performed identically to the first set and loaded at room temperature in a RTP furnace. A surface pre-treatment consisting of an in-situ RTA step was carried out in H_2 at 800ºC for 2 min to improve the interface quality [45]. The gate oxide was formed by RTO under the same conditions as in the first set of MOSFETs but for 5 min, resulting in a thinner oxide (30 nm). Post-oxidation annealing was also carried out during 3 min. On top of this thermal oxide, a 52 nm TEOS oxide was deposited [Fig 3.8.b]. At the end of the process, the total gate oxide layer is about 82nm (30 nm RTP N_2O + 52 nm TEOS).

Table 3.2 summarized the main details of gate oxidation processes. After the oxide formation of both set of MOSFETs, a 150 nm Ni layer was sputtered to form the source/drain contacts and then annealed in Ar at 1100ºC for 2 min. A 500 nm thick Al layer was sputtered and not annealed for the gate electrode. The fabricated MOSFETs#1 and #2 did not show any

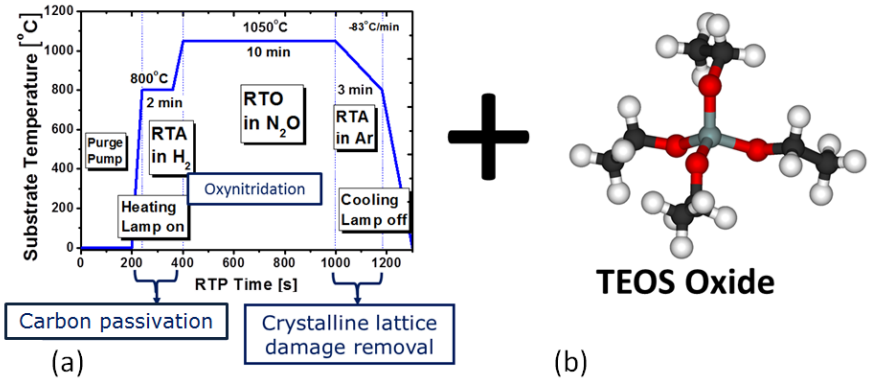


Fig.3.8. Oxinitridation process, including the role of each step for MOSFETs#1 samples fabrication (a). MOSFETs#2 used the same process but with a different cleaning temperature. At the end of the thermal oxidation process, a TEOS oxide is deposited (b).

EP improvement compared to the state-of-the-art EP since their gate oxides have been designed with the aimed to study the 4H-SiC MOSFETs irradiation harshness. The poor gate oxide quality makes easier to reveal the particle irradiation. impact on the EP MOSFETs, leading to qualitative and explicit conclusions. Once the fabrication process was completed, the devices were electrically characterized and prepared for irradiation. The wafers were diced into dies, pasted on Si wafer with carbon tape, and sent for the irradiation experiments.

MOSFETs	H_2	N_2O	Ar	Deposited TEOS
#1	[900ºC;2min]	[1050ºC; 10min] T_{OX} = 38nm	[1050ºC→22ºC] Ramp down	None
#2	[800ºC;2min]	[1050ºC; 5min] T_{OX} = 30nm	[1050ºC→22ºC] Ramp down	52 nm T_{OX} = 82nm

Table 3.2 Growth parameter and condition detail of the different gate oxide MOSFETs

3.3.2.3 Irradiation set-up

Once completed the fabrication process and performed the first devices' electrical characterization, the irradiation of all the SiC-MOSFETs were carried out at the Helmholtz-Zentrum Dresden-Rossendorf (HZDR) without biasing the devices and at room temperature. 15 Si wafers containing 2 individual dies were irradiated with protons and electrons at various energies and fluences (see Table 3.1). Each die includes 80 lateral MOSFETs (MOSFETs#1 and #2) with different gate lengths and widths, and 4 MOS capacitors. After irradiation, the SiC-MOSFETs were electrically characterized and post-annealed under N_2 at 120ºC for 14, 84 and 154 h to study the recovery mechanism, as it is typically carried out in Si-MOSFETs. The MOSFETs were measured before irradiation, after irradiation and after each annealing step, using the BSI technique and following the cycle defined in section 2.6. After the final annealing, they were measured under BTI, from 25ºC to 250ºC and presented also in the next chapter. In this chapter, the apparent field effect mobility (μ_{fe}), the threshold voltage after a positive (V_{TH_PBSI}), negative bias stress (V_{TH_NBSI}), the threshold voltage hysteresis (ΔV_{TH} = V_{TH_NBSI} - V_{TH_PBSI}), the effective oxide and interface charge number brought by the BSI stress $|N_{ox}+N_{it}|$, and sub-threshold current of irradiated MOSFETs were furthermore extracted from the I_{DS} (V_{GS}) characteristics, and compared with those of non-irradiated (NI) MOSFETs. Moreover, the I_{DS} (V_{DS}) characteristics were also measured.

The next sections describe the MOSFETs behaviour before and after irradiation at low, medium and high energies. For the sake of clarity, the adopted approach consists in showing:

1 → $I_{DS}(V_{GS})$ curves after each irradiation fluence together with the gate leakage and field effect mobility variation.

2 → $I_{DS}(V_{GS})$ curves subjected to BSI test for a chosen fluence value, and their comparison with those of non-irradiated MOSFETs.

3 → V_{TH_NBSI}, ΔV_{TH} and the GIDL current time evolution for the different fluences.

4 → The table of the main EP values.

The interface trap density of 4H-SiC irradiated and non-irradiated MOSFETs is not evaluated in this chapter, and it will be presented in chapter 6 for the case of a higher quality of gate oxide. The presented results have been obtained on 4 different MOSFETs that, before irradiation, after irradiation in similar irradiation conditions have shown similar behaviour.

3.4. Proton irradiation of MOSFETs with N_2O Gate oxide

The EP presented below accounts for devices with a gate length (L) and width (W) of L/W = 12 µm /150 µm.

3.4.1. Low-Energy proton Irradiated MOSFETs

MOSFETs irradiation under low proton energy (in this case 0.18 MeV) allows studying their electrical behaviour when the proton beam stops into the P-epilayer and releases its energy. In a first approach, experimental I_{DS} (V_{GS}) characterization has been carried out. The comparison between the NI samples and the irradiated ones allows studying the impact of both the generated traps and the ion mobile charges in the oxide on the V_{TH} shift.

Effect of radiation fluence on the transconductance

Fig. 3.9.a shows the experimental I_{DS} (V_{GS}) curves for different fluence values. As it can be seen, there is a remarkable negative shift of the transconductance curves as the fluence value is increased up to $5x10^{12}$ cm^{-2}. This negative shift could be caused by the fact that donor traps generated by irradiation at or near the SiO_2/SiC interface predominate over the acceptor traps. It is well known that these donor states can trap a certain amount of holes either generated during the irradiation process and have reached the SiO_2/SiC interface, or coming from the p-epilayer. The increment of positive charge in the oxide induces a negative shift of the transconductance characteristic, lowering the threshold voltage value. As the I_{DS} (V_{GS}) measurement is performed from -12V to +12V after irradiation, the trapping event may be more efficient since the gate is negatively biased. However, the transconductance shift changes from negative to positive as the fluence value is increased. Concretely, for a fluence of $5×10^{13}$ cm^{-2} the transconductance curve is very closed to the NI samples. This fact indicates that the amount of generated acceptor traps at or near the SiO_2/SiC interface start to equalize the amount of generated donor traps. As a consequence, V_{TH} shifts toward more positive values compared with that of low fluence irradiated sample. Hence, it is predicted that a higher concentration fluence may induce a positive shift of the threshold voltage, this fact been experimentally confirmed in chapter 6. Moreover, these low energy irradiation experiments have shown the absence of rebound effect. The V_{TH} values after two years with some post irradiation annealing treatment remain below the V_{TH} value of the NI sample.

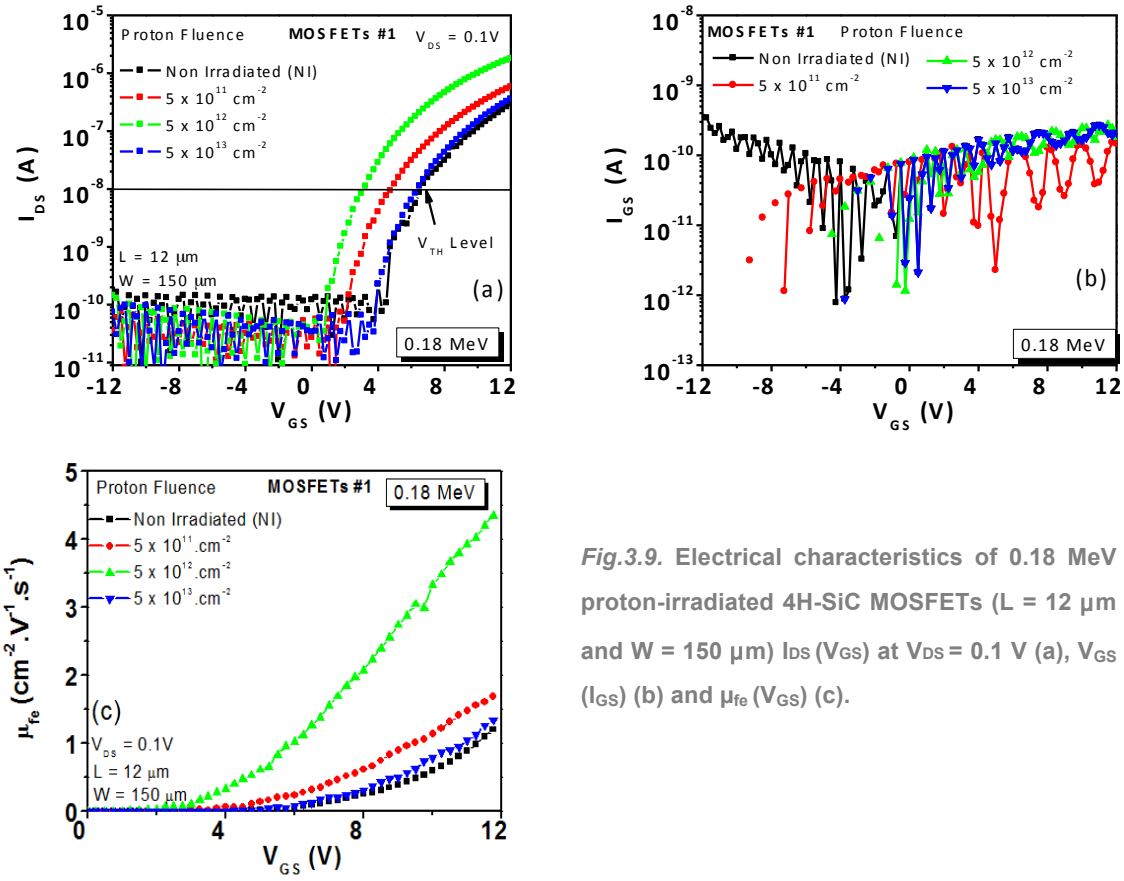


Fig.3.9. **Electrical characteristics of 0.18 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), V_{GS} (I_{GS}) (b) and μ_{fe} (V_{GS}) (c).**

Impact on channel carriers mobility and leakage current

The most surprising result of these experiments is the apparent increase of the channel carrier mobility μ_{fe} [Fig.3.9.c] after irradiation. These results may be justified by hypothesises related to nitrogen diffusion, hydrogen atom creation at the epilayer, and charge compensation at the SiO_2/SiC interface. This is discussed in (section 3.4.5). In addition, the mobility dependence on irradiation fluence seems to have a shift as in the case of V_{TH}; i.e., μ_{fe} increases with fluence values and for a high fluence starts to decrease approaching to the NI sample value. Moreover, the I_{GS} (V_{GS}) characteristics show the absence of relevant gate leakage current [Fig.3.9.b]. This fact is in contradiction with what has been founded in Si MOSFETs state-of-the-art [46-47]. The absence of relevant leakage current accounts for a high robustness of the oxynitrided gate oxide used in the fabricated SiC MOSFETs.

Bias stress instability tests

When comparing I_{DS} (V_{GS}) experimental curves of the NI sample [Fig.3.10.a] with the irradiated one at a proton fluence of $5 \cdot 10^{12}$ cm^{-2} after a time BSI [Fig.3.10.b], the first observation is the clear decrease of the threshold voltage hysteresis when sweeping V_{GS} from negative to positive and vice-versa. Indeed, the gap between V_{TH_NBSI} and V_{TH_PBSI} is reduced after proton irradiation and the drift became slightly negative, contrarily to non-irradiated devices.

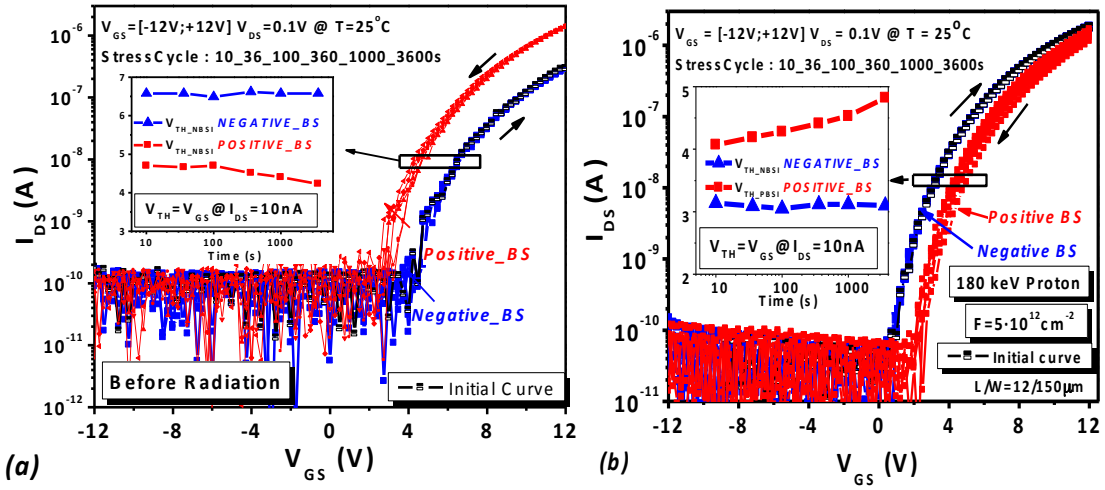


Fig. 3.10. n-MOSFET Threshold voltage evolution versus time during the BSI test. (a) For a non-irradiated sample and (b) for a 180 keV $5 \cdot 10^{12}$ cm^{-2} proton irradiated MOSFET. Positive BS: The bias gate voltage switches from positive to negative values. Negative BS: The bias gate voltage switches from negative to positive values.

This fact confirms the predominance of the donor state traps in the oxide interface generated by the irradiation. When these donors state traps accumulate at the SiO_2/SiC interface during the negative gate bias, they overcompensate the exceeding acceptor traps at the SiO_2/SiC interfaces and then trap holes coming from the epilayer by charge tunneling, this accounting for the ΔV_{TH} negative shift. As observed in Fig 3.11.a, the V_{TH_NBSI} is stable with stress time and this stability is not impacted by the irradiation process. Furthermore, the threshold voltage drift ΔV_{TH} of the irradiated devices has been clearly reduced after irradiation, being closer to 0V. Fig.3.11.b. It can also be observed that the ΔV_{TH} time stability is slightly improved after irradiation, especially for the highest fluence value. This low and stable hysteresis is synonym of very few amounts of effective oxide and interface charges. To represent this amount of charges, we defined the $|N_{it} + N_{ox} \times 10^{12}|$ parameter (see chapter 2). This parameter has been calculated with experimental ΔV_{TH} values at the beginning of bias stress, as indicated in Fig. 3.11. b. For instance, at a radiation fluence of $5 \cdot 10^{13}$ cm^{-2}, the effective charge amount is reduced by one order of magnitude in comparison with the NI MOSFET (see Table 3.3). This parameter is just an approximation in the sense that not all the N_{it} and N_{ox} generated are detected during measurement, due to the fact that some of the charges compensate to each-other. The ΔV_{TH} sign determine the polarity of the charges brought at the SiO_2/SiC interface during the BSI stress. If $\Delta V_{TH} < 0$, charges predominating at the interface are donor-type. They are acceptor-type when $\Delta V_{TH} > 0$. As the hysteresis amplitude is slightly negative for all fluences, the polarity of the charge moving at the interface during the positive bias stress is negative.

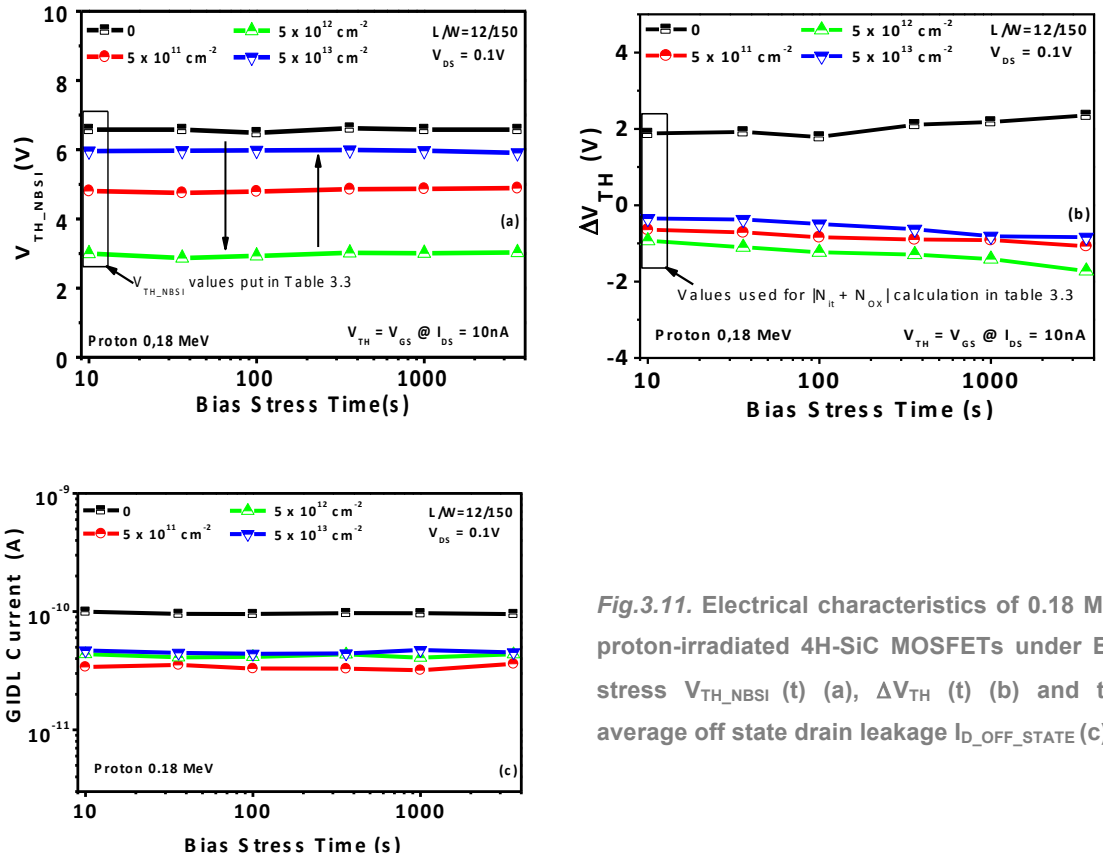


Fig.3.11. **Electrical characteristics of 0.18 MeV proton-irradiated 4H-SiC MOSFETs under BSI stress V_{TH_NBSI} (t) (a), ΔV_{TH} (t) (b) and the average off state drain leakage $I_{D\_OFF\_STATE}$ (c).**

GILD current

Moreover, the GIDL current [Fig.3.11.c] present negligible variations, accounting for no critical damage of the irradiation beam at the epilayer surface. The GIDL current typically indicates a two-step tunneling mechanism which is hole tunneling from interface traps to a valence band (step 1) and electron tunneling from the traps to a conduction band (step 2), forming a complete and major leakage path, and typically leading to drain leakage currents in Si off-state MOSFET's [48-50]. GILD current did not appear in any of the present irradiated SiC devices, denoting the SiC MOSFET radiation hardness.

Other parameters

Additionally, the oxide breakdown voltage V_{oxide_br} is also not significantly impacted by the irradiation process and even show a small improvement versus non-irradiated oxide (see Table 3.3). V_{oxide_br} has been defined as the gate voltage at which the leakage current overcomes 10 nA. Moreover, the irradiation didn't impact the contact resistance for any of the irradiated samples at all energies. The maximum drain saturation values ($I_{D\_SAT\_MAX}$) extracted at V_{DS}=10V and V_{GS}=12V are also reported in Table 3.3. Note that the value obtained after an irradiation fluence of $5 \cdot 10^{11}$ cm^{-2} does not fit with the μ_{fe} increase. However, we must remind that the μ_{fe} values have been extracted at V_{DS}=0.1 V, while the saturation current is obtained at high drain voltages at which additional scattering mechanisms highly lower the μ_{fe} value. The impact of irradiation on MOSFETs operating at high V_{DS} has not been studied in the frame of this thesis. A maximum value of mobility and saturation current is obtained for the intermediate fluence of

Electrical Parameters	Non Irradiated	Proton Energy: 0.18 MeV		
		$5{\cdot}10^{11}$ cm^{-2}	$5{\cdot}10^{12}$ cm^{-2}	$5{\cdot}10^{13}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ (V)	6.58	4.89	3.1	5.96
V_{oxide_br} (V)	23.42	31.46	26.54	26.02
$\mu_{fe\_Vg=12V}$ (cm^2.V^{-1}s^{-1})	1.05	1.57	5.00	1.03
$I_{D\_SAT\_MAX}$ (µA)	15.33	6.92	29.11	8.62
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert$(cm^{-2})	1.06	0.36	0.52	0.19

Table 3.3 4H-SiC n-MOSFET main electrical parameters before and after 0.18 MeV proton irradiations at three different fluences.

$5{\cdot}10^{12}$ cm^{-2}. Then, we could conclude that this fluence is the optimum value for improving the oxynitrided gate MOSFETs performances using low energy proton irradiation. In any cases, it can be guarantee that proton irradiation at low energy do not negatively impact the MOSFETs properties at room temperature when fluence varies up to $5{\cdot}10^{13}$ cm^{-2}. However, above this fluence value, the MOSFET electrical parameters tend to degrade as we will show in chapter 6.

Time annealing impact

For PIA MOSFETs irradiated with fluences of $5{\cdot}10^{11}$ [Fig 3.12.a] and $5{\cdot}10^{12}$ cm^{-2} [Fig 3.12.b], the annealing tends to induce V_{TH_NBSI} recovery: the longest the annealing time, the closer the V_{TH_NBSI} to the NI values (better recovery). However, for a fluence of $5{\cdot}10^{11}$ cm^{-2} after 154h, V_{TH} and ΔV_{TH} values have shown a significant increase with stress time [Fig 3.12.a and 3.13.a]: This increase is much higher than that of the NI MOSFET under BSI measurement. It indicates a predominance of acceptor traps after the annealing process during the BSI stress. To explain such a behavior, we suggest that during the annealing process not only the e-h recombination can occur. A lot of mechanisms have to be taken into consideration. They are all detailed in section 4.2.3. In this case, it is suggested that the predominant one is the electron charge trapping at the SiO_2/SiC interface during annealing. At this irradiation energy, this charge trapping effect strongly depends on the fluence value and perhaps on the oxide thickness. For this fluence ($5{\cdot}10^{11}$ cm^{-2}), μ_{fe} has not shown any visible change either before or after the proposed annealing time [Fig 3.14.a].

PIA MOSFETs irradiated at F = $5{\cdot}10^{12}$ cm^{-2}, V_{TH} and ΔV_{TH} [Fig 3.12.b and 3.13.b] has firstly shown a decreasing tendency with a short annealing time before starting the recovery toward its initial value before irradiation. The surprising results have shown a 10% increase of the μ_{fe} after annealing in comparison with the irradiated MOSFETs [Fig 3.14.b]. This behaviour suggests that the nitrogen diffusion is predominant over the other mechanisms, because the V_{TH} stability is maintained during the recovery, and μ_{fe} has also increased after annealing [Fig 3.14.c]. Indeed, we believe that the annealing process may induce a deeper diffusion of the passivating species in the epilayer, just enough to prevent the tunneling of the mobile ion charge located in the epitaxial layer nearby the SiO_xN_y transition layer (keeping the V_{TH} stability)

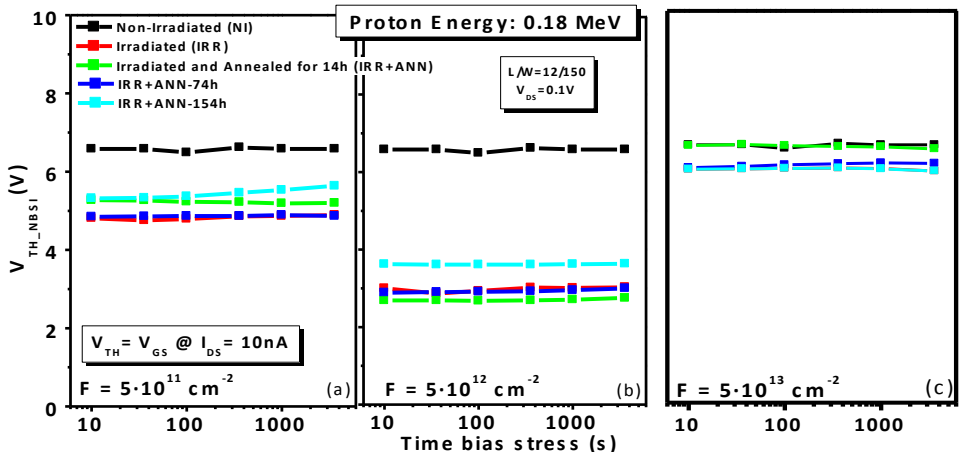


Fig 3.12. The threshold voltage time evolution after a NBS for 0.18 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

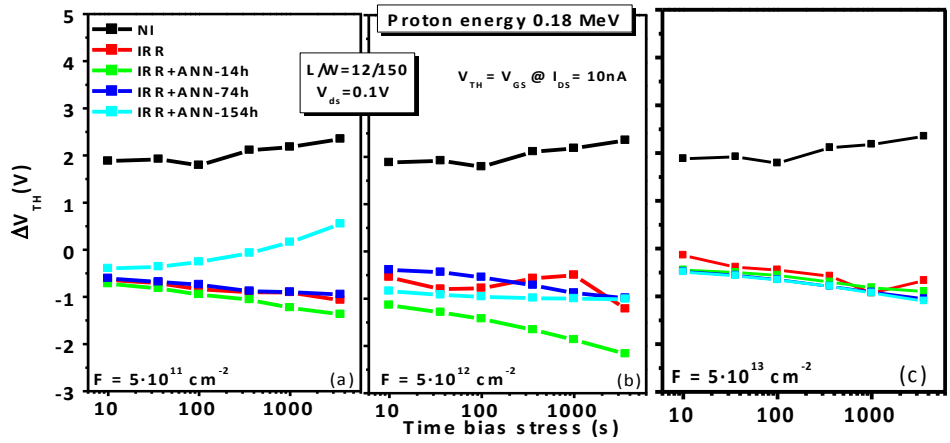


Fig 3.13 The threshold voltage hysteresis time evolution for 0.18 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

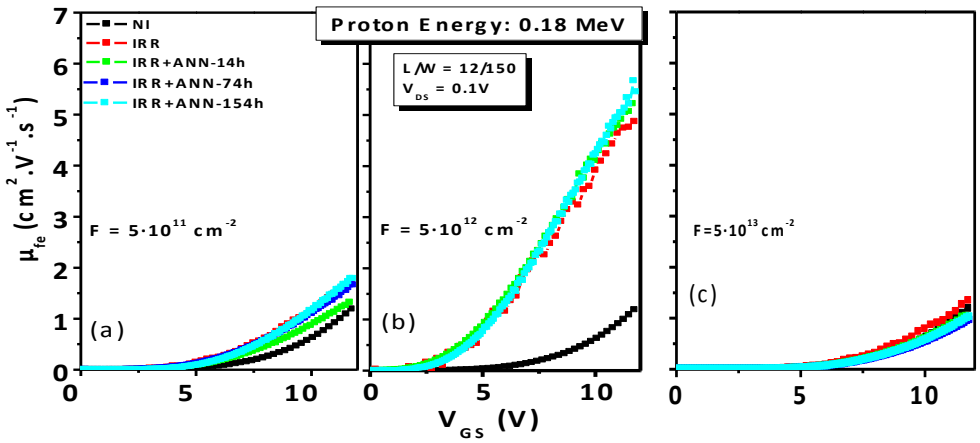


Fig 3.14. The field effect mobility time evolution after a 0.18 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}\ cm^{-2}$ (a), $5{\cdot}10^{12}\ cm^{-2}$ (b) and $5{\cdot}10^{13}\ cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

0.18 MeV Proton Fluence (p/cm^2)	NI*	$5 \cdot 10^{11}$		$5 \cdot 10^{12}$		$5 \cdot 10^{13}$	
		IRR*	ANN*	IRR	ANN	IRR	ANN
$V_{TH\_NBSI\_t=10s}$ (V)	6.6	4.9	5.3	3.1	3.6	6.47	5.96
V_{oxide_br} (V)	23.4	31.4	30.4	26.5	26.3	26.0	26.1
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	1.20	1.6	1.7	5.0	5.6	1.3	1.25
$I_{D\ SAT\ MAX}$ (µA)	15.04	6.9	6.18	29.1	31.5	8.6	12.23
$\lvert N_{ox} + N_{it} \rvert$ x 10^{12} cm^{-2}	1.06	0.36	0.22	0.52	0.47	0.19	0.27

Table 3.4. The extracted electrical parameters on irradiated at 0.18 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#1. NI= MOSFETs measured prior to irradiation, IRR = MOSFETs measured after irradiation and ANN = MOSFETs measured after 154h of post irradiation annealing.

while slightly increasing the μ_{fe}. Nevertheless, for the highest fluence, it seems that the V_{TH_NBSI} [Fig 3.12.c] and μ_{fe} [Fig 4.4.c] recover to their initial values whereas ΔV_{TH} remained unchanged [Fig 3.13.c]. The lower μ_{fe} values compared with the previous fluence suggest higher lattice damage near the interface. As for the medium fluence case, we expect a predominant role of nitrogen diffusion during the annealing due to the V_{TH} stability. In any cases, and for each irradiated MOSFET at all energies, the other electrical parameters like GIDL current, gate-source leakage current and oxide breakdown voltage values didn't show any changes of their values before annealing, meaning that the annealing time up to 154h didn't impact any of the PIA MOSFETs from the leakage point of view. The variation of the main electrical parameters of the NI MOSFETs, irradiated MOSFETs and PIA MOSFETs after 154h are indexed in Table 3.4. For the sake of clarity, all the tables related with the study of PIA MOSFETs#1 irradiated at all fluences and energies have been indexed together. They can be founded after the study of PIA MOSFETs#1 irradiated at 15 MeV.

3.4.2. Medium energy proton irradiated MOSFETs

Effect of radiation fluence on the transconductance

MOSFETs medium energy proton irradiation (between 1 MeV and 8.5 MeV) allows studying its electrical behaviour when the proton beam stops and releases its energy inside the SiC N^+ bulk. The proton beam damages the oxide and the SiC bulk. The negative shift of the transconductance curves previously seen at low proton energy is also observed [Fig.3.15.a]. However, the V_{TH} keeps on drifting more and more toward the negative values when the fluence is increased, and reach its maximum negative value at an irradiation fluence of 5×10^{14} cm^{-2}. The medium irradiation energy creates donor and acceptor traps in the oxide and in the SiC substrate. However, in this case the donor state traps generated by irradiation predominate at the SiO_2/SiC interface over the acceptor ones for all irradiation fluences in contrast to what happened for low irradiation energies. In all fluence cases, the gate current leakage didn't show any changes with the irradiation [Fig.3.15.b] and remains very low. This behaviour is exactly the same than that reported for the low energy case. Regarding channel carrier mobility, μ_{fe} increases with the fluence value following the V_{TH} negative drift behaviour. Concretely, μ_{fe} at a

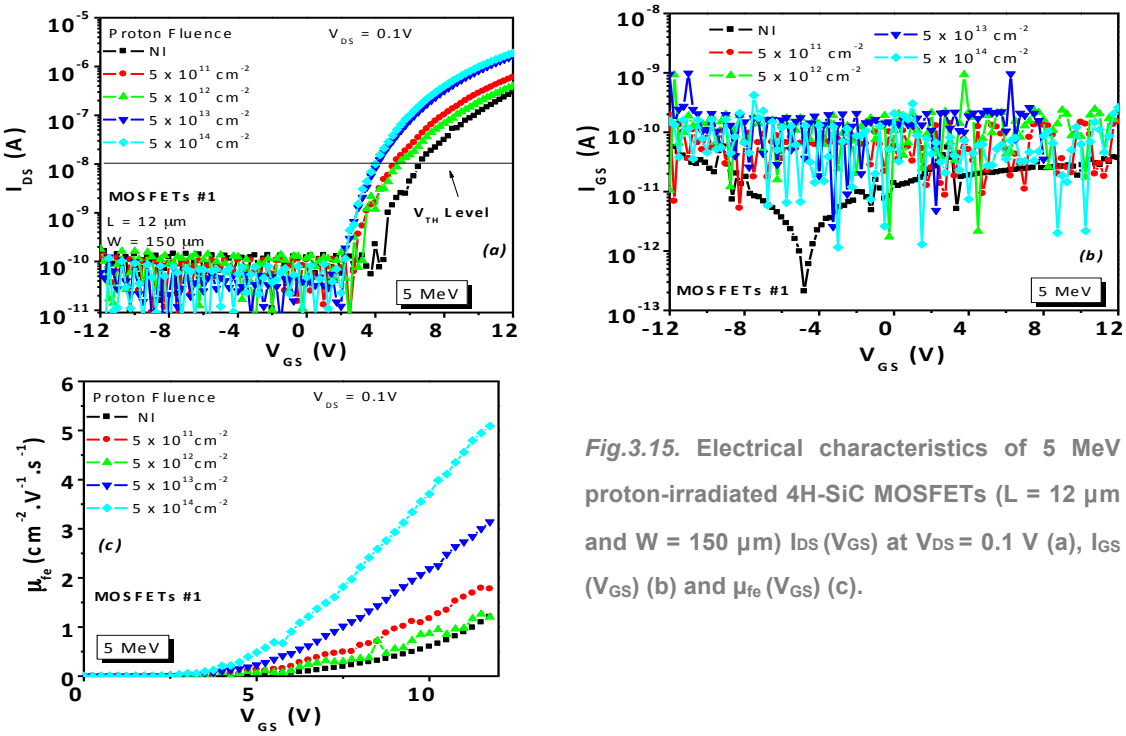


Fig.3.15. **Electrical characteristics of 5 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b) and μ_{fe} (V_{GS}) (c).**

fluence of 5 × 10^{14} cm^{-2} is four times [Fig.3.15.c] the value obtained in the NI MOSFETs, possibly due to the nitrogen diffusion (section 3.4.5).

BSI tests

Fig. 3.16 a and b shows the transfer characteristics instability of the MOSFET irradiated at 5·10^{14} cm^{-2} fluence as a function of the **s**tress time after the BSI measurement. Similar behaviour of the transconductance characteristics and ΔV_{TH} is observed as in 3.3.1 (180KeV proton irradiation):

- Under NBSI, the irradiated MOSFETs start to conduct at lower gate threshold voltage than the NI ones.
- It can be observed that the I_{DS} (V_{GS}) curves exhibit almost the same on-state drain currents after either positive bias stress (PBS) or negative bias stress (NBS) for all the irradiated samples.
- The V_{TH_NBSI} curves of SiC MOSFETs irradiated with all fluences [Fig.3.17.a] show acceptable time stability, especially for fluence values up to 5·10^{13} cm^{-2}.

On the other hand, ΔV_{TH} is quite stable with time for all fluences as it is also true for the NI samples. However, the amplitude is closer to 0V for all fluences compared to the NI samples [Fig.3.17.b]. The optimum V_{TH} and ΔV_{TH} stability is reached for MOSFETs irradiated at a fluence of 5·10^{13} cm^{-2}, and the introduced interface and oxide traps due to the BSI stress is 3 times lower than in the NI case (see Table 3.4). However, at an irradiation fluence of 5·10^{14} cm^{-2} (and despite the μ_{fe} increase), the MOSFETs V_{TH} time stability starts to degrade after 1 hour of bias stress time, becoming worse than the NI MOSFETs.

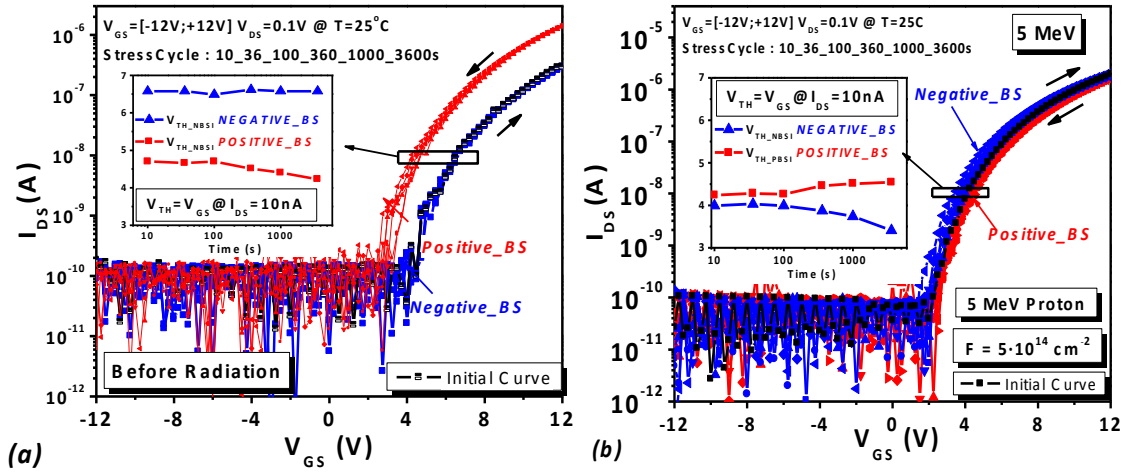


Fig. 3.16. n-MOSFET Threshold voltage evolution versus time during the BSI test. (a) For a non-irradiated sample and (b) for a 5 MeV $5 \cdot 10^{14}$ cm^{-2} proton irradiated MOSFET

The GIDL current [Fig.3.17.c] shows negligible changes, being mainly unaffected by proton irradiation. The main electrical parameters extracted from this 5 MeV irradiation experiment are summarized in (Table 3.5). As observed in previous paragraph, the MOSFET oxide breakdown voltage increased after irradiation. However, at high irradiation fluences, this increase is much important than those observed in the low energy proton irradiated case. Regarding drain energies (see section 3.4.1). For all the irradiation fluences, the irradiation

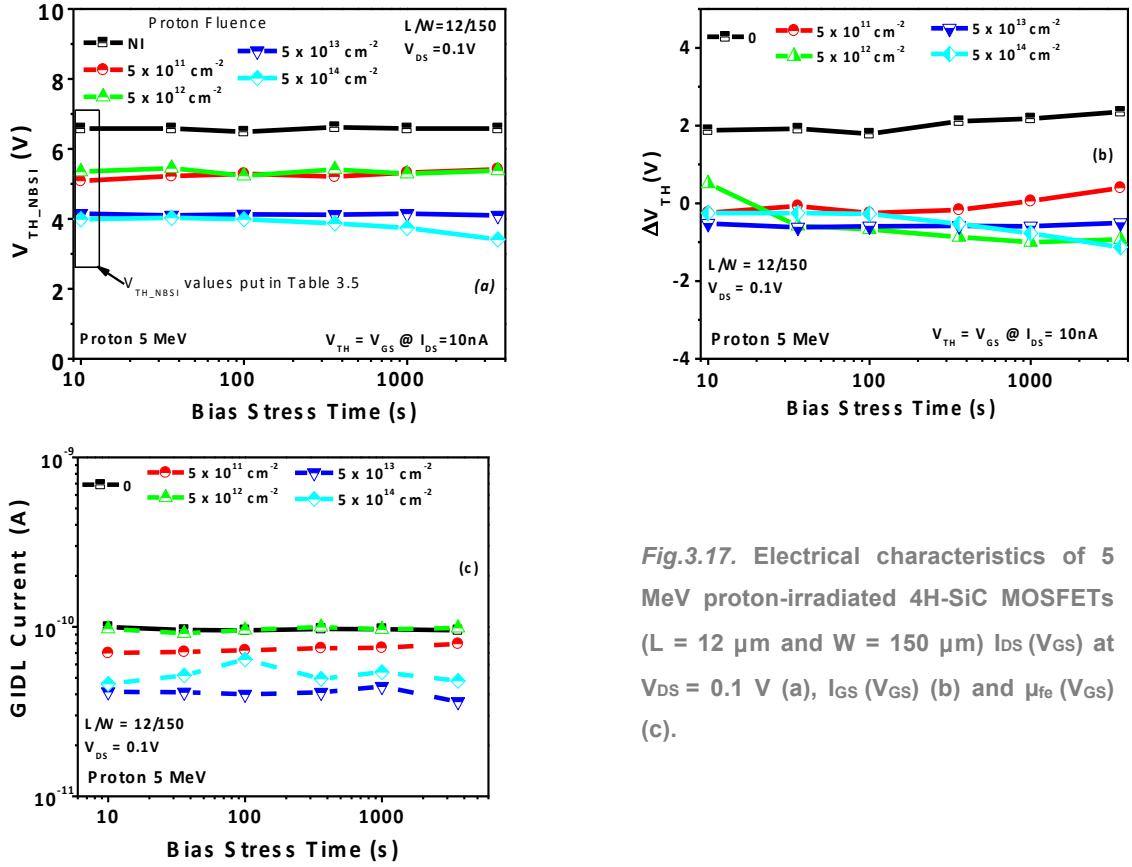


Fig.3.17. Electrical characteristics of 5 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b) and μ_{fe} (V_{GS}) (c).

harshness of the oxynitrided gate oxide is demonstrated in the sense that neither GIDL nor gate leakages are detected after irradiation at all fluences. In addition, the EPs have not been negatively impacted by the irradiation.

Electrical Parameters	Non Irradiated	Proton Energy: 5 MeV			
		$5{\cdot}10^{11}$ cm^{-2}	$5{\cdot}10^{12}$ cm^{-2}	$5{\cdot}10^{13}$ cm^{-2}	$5{\cdot}10^{14}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ [V]	6.58	5.09	5.35	4.25	3.99
V_{oxide_br} [V]	23.42	23.6	30.2	29.15	26.41
$\mu_{fe\_Vg=12V}$ [cm^2.V^{-1}s^{-1}]	1.20	1.71	1.40	3.29	5.20
$I_{D\_SAT\_MAX}$ [µA]	15.33	5.64	10.90	22.51	34.04
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert$[cm^{-2}]	1.06	0.11	0.28	0.34	0.11

Table 3.5. 4H-SiC n-MOSFET main electrical parameters before and after 5 MeV proton irradiations at four different fluences.

Time Annealing impact

For the $5{\cdot}10^{11}$ cm^{-2} fluence, V_{TH_NBSI} of the PIA MOSFETs has shown slightly higher values than that of the irradiated MOSFETs, moving towards the non-irradiated values as the annealing time is increased [Fig 3.18]. However, it seems that even a long annealing time does not induce a strong V_{TH_NBSI} recovery. Even after 154 h of PIA, the irradiated nMOSFETs V_{TH_NBSI} increased by 0.3V in comparison with the value before PIA. In the case of the PIA MOSFETs irradiated with a fluence of $5{\cdot}10^{12}$ cm^{-2}, V_{TH_NBSI} didn't show any significant changes [Fig 3.18.b]. However in the case of the irradiated MOSFETs at a fluence of $5{\cdot}10^{13}$ cm^{-2}, V_{TH_NBSI} has shown a curious variation. Indeed, with the increase of the annealing time, the V_{TH_NBSI} of the PIA MOSFET firstly decreased before totally recover to the V_{TH_NBSI} value of the irradiated MOSFETs and not to the NI MOSFETs [Fig 3.18.c]. This decrease may be justified by a predominance of additional electrons that are being detrapped with the annealing time, and accumulate at the SiO_2/SiC interface during the annealing over the other phenomenon. It quickly disappears after a long annealing time due to either the recombination process or, another charge trapping effect. At a first sight, PIA V_{TH_NBSI} of MOSFET irradiated at $5{\cdot}10^{14}$ cm^{-2} presented a drift that fluctuates in a non-lineary way, nearby the irradiated value [Fig 3.18.d]. However, the V_{TH_NBSI} time stability has been improved, and, contrary to the irradiated MOSFETs, is more stable at long time stress. The PIA process improved the ΔV_{TH} long time stability behavior of the irradiated MOSFETs [Fig 3.19.a, b, c and d]. The type of residual N_{ox} + N_{it} charges brought at the SiO_2/SiC interface remains negative along the stress, and do not change to positive, meaning that the holes could have either recombined with an electron or fall into an donor trap located in the oxide layer during the annealing process. Their initial values can be founded in table 3.6. The main difference with the PIA at 0.18 MeV is that the epilayer in

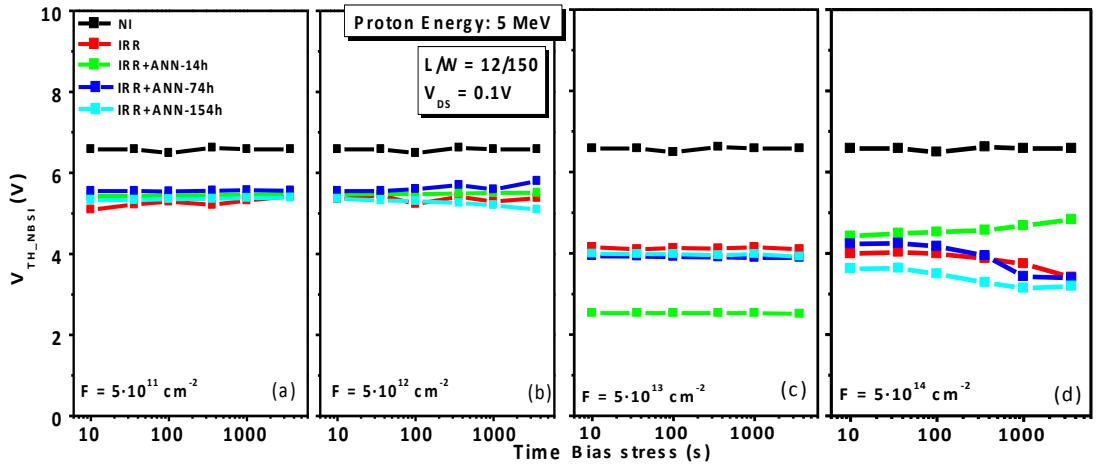


Fig 3.18. The threshold voltage time evolution after a NBS for 5 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b), $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

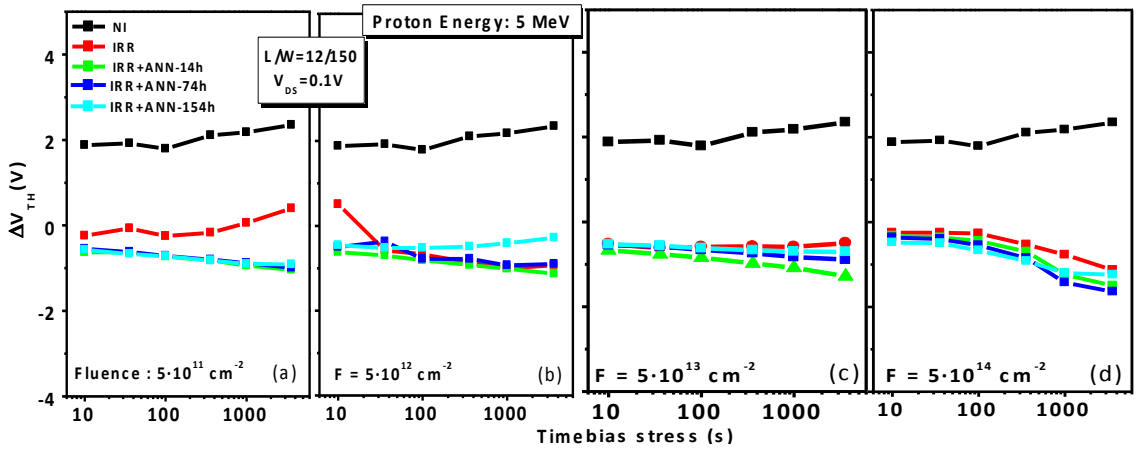


Fig 3.19. The threshold voltage hysteresis time evolution for 5 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}\,cm^{-2}$ (b) $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

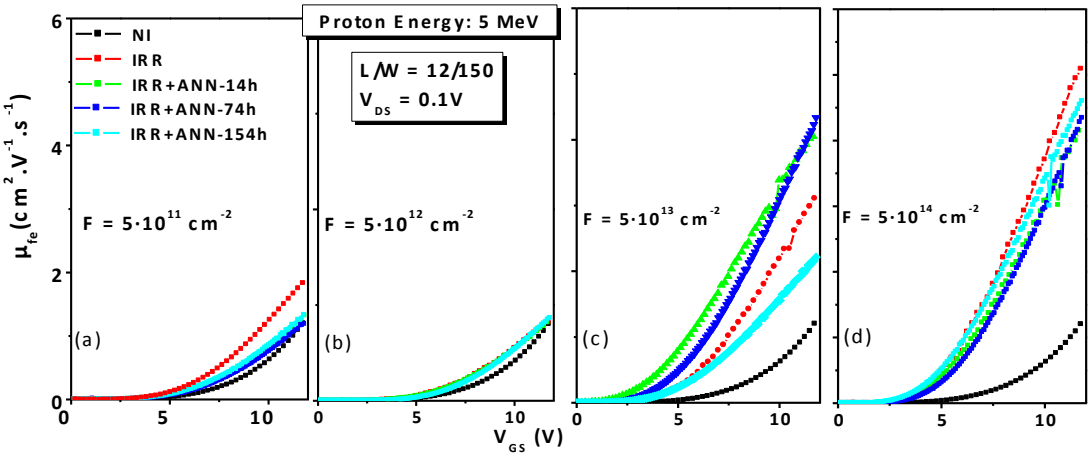


Fig 3.20. The field effect mobility time evolution after a NBS for 5 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}\,cm^{-2}$ (b) and $5{\cdot}10^{13}\,cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

5 MeV Proton Fluence (p/cm^2)	NI	$5\cdot10^{11}$		$5\cdot10^{12}$		$5\cdot10^{13}$		$5\cdot10^{14}$	
		IRR	ANN	IRR	ANN	IRR	ANN	IRR	ANN
$V_{TH\_NBSI\_t=10s}$ (V)	6.58	5.09	5.2	5.35	5.32	4.15	3.99	3.99	3.62
V_{oxide_br} (V)	23.4	23.6	23.4	30.2	29.8	29.1	29.1	26.4	26.3
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	1.20	1.77	1.32	1.20	1.29	3.10	2.21	5.09	4.60
$I_{D\_SAT\_MAX}$ (µA)	15.04	11.02	3.88	5.60	10.9	22.91	23.8	34.30	28.7
$\lvert N_{ox} + N_{it} \rvert$ x 10^{12} cm^{-2}	1.06	0.11	0.32	0.28	0.26	0.34	0.31	0.11	0.37

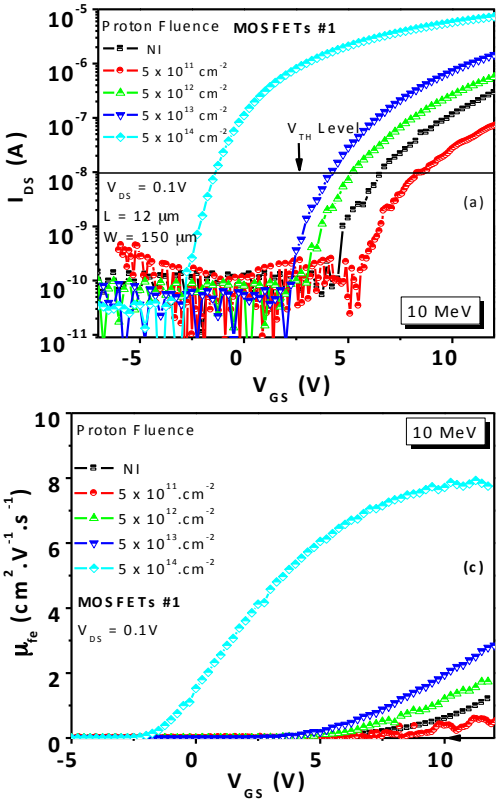
Table 3.6. The extracted electrical parameters on irradiated at 5 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#1.

this case is not really impacted by the irradiation, because the proton beam crossed it before stopping deeply into the substrate. Thus, a small contribution of the e-h generated at the epilayer can enter at stake. In addition, higher μ_{fe} values are measured at the high fluence values in contrast to the previous experiments at 0.18 MeV. We have also observed that, for MOSFETs irradiated under the lowest [Fig 3.20.a] and highest fluence [Fig 3.20.d], the extracted μ_{fe} after the PIA have shown a recovery tendency, decreasing their value with the increase of the annealing time, slightly recovering to the NI value. For the $5\cdot10^{12}$ cm^{-2} fluence [Fig 3.20.b], μ_{fe} seems to be unaffected whereas for the $5\cdot10^{13}$ cm^{-2} fluence increases a 30% approximately after a short annealing time [Fig 3.20.c], before abruptly recover to the non-irradiated values at longer annealing time. The μ_{fe}, together with the V_{TH_NBSI} turnover that occurred in this case ($5\cdot10^{13}$ cm^{-2} fluence) may suggest that, at 120°C, it may exist a threshold annealing time (T_{th}), from which the recovery of the electrical parameter starts to be really visible. This T_{th} may be a function of temperature, but also of the amount of interface and oxide charges that have been generated by the irradiation within the oxide. At the highest fluence, μ_{fe} has shown a very slow recovery tendency, not very significant to consider that a "true annealing" has been occurred. The V_{oxide_br} didn't present any variation even after a long time annealing, confirming the good irradiation harshness of PIA MOSFETs.

3.4.3. High energy proton irradiated MOSFETs

Effect of radiation fluence on the transconductance

In this next experiment, the analysis has been performed on irradiated sample having the proton beam energy high enough to crossing the entire MOSFETs die thickness (10 MeV). This energy is the theoretical irradiation energy limit before nuclear reaction occurs [5]. The electrical behaviour of the irradiated MOSFETs seemed to follow a similar behaviour to the medium energy irradiation. The main difference when compared to the NI MOSFET values is that the transconductance characteristics of irradiated devices firstly increased with the fluence, before shifting toward negative values at highest fluence [Fig 3.21.a]. However, the large MOSFET leakage current for a fluence value of $5\cdot10^{11}$ cm^{-2} (one order of magnitude higher than that obtained in the other MOSFETs) indicates a non-proper electrical behaviour of the device.



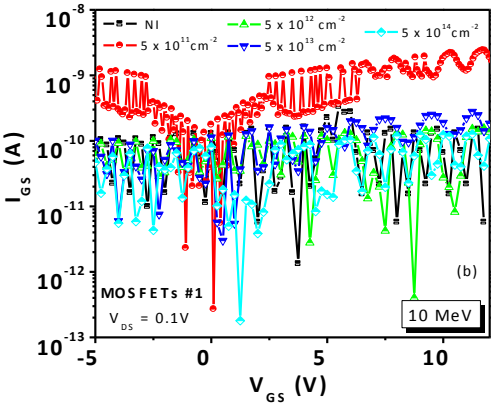


Fig. 3.21. **Electrical characteristics of 10 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b) and μ_{fe} (V_{GS}) (c).**

Consequently, the transconductance behaviour can be considered similar to the case of medium energy irradiation if neglecting the irradiated case with the lowest fluence value.

The gate leakage is kept below 0.2 nA in all cases except for a fluence value of $5 \cdot 10^{11}$ cm^{-2} [Fig 3.21.b]. The irradiated MOSFETs main EPs extracted from the experimental characteristics are shown in Table 3.7. The apparent μ_{fe} presents, neglecting the lowest fluence case, a significant increase with the fluence [Fig.3.21.c]. Indeed, at the highest irradiation fluence, μ_{fe} has even been multiplied by a factor of 6 compared to the NI value. In addition, the mobilities values after the 10MeV irradiation step are higher than those obtained after a 5 MeV irradiation for a fluence of $5 \cdot 10^{14}$ cm^{-2}. At this fluence, the maximum I_{DSAT_MAX} at V_{GS}=12V is increased by a factor of 15 and the transconductance g_m becomes more than 6 times (like μ_{fe}) higher with respect to the NI MOSFETs values. However, V_{TH} has become highly negative (< -1V) and the device becomes normally-on.

BSI stress

Similarly to previous samples, BSI tests have been performed. Fig.3.22.a and Fig.3.22.b are showing the I_{DS} (V_{GS}) characteristics evolution with stress time, before and after irradiating with $5 \cdot 10^{13}$ cm^{-2} proton fluence. During these experiments, we have evidenced that when the fluence increases, the V_{TH_NBSI} tends to decrease [Fig.3.23.a], while μ_{fe} increases. Neglecting the $5 \cdot 10^{11}$$cm^{-2}$ case, no change of the predominant interface trap type is denoted: the higher the irradiation fluence, the higher the amount of donor is brought at the SiO_2/SiC

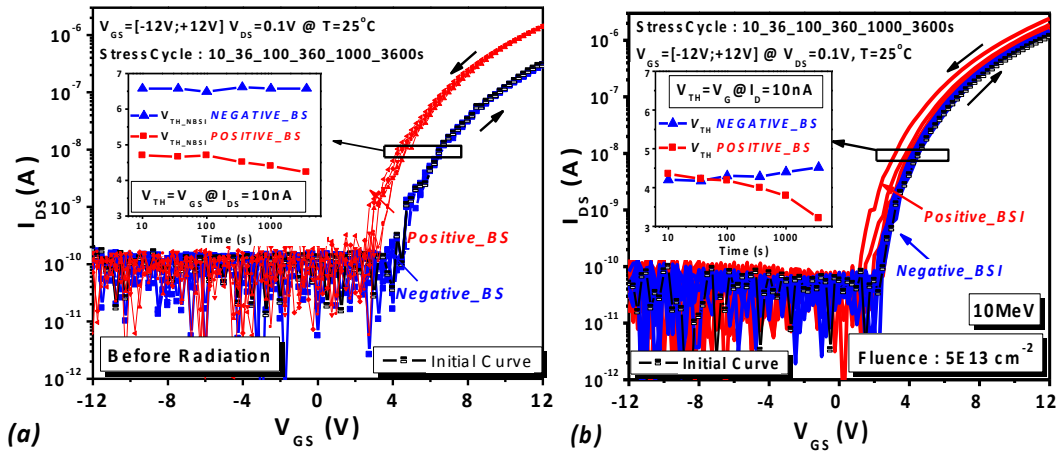


Fig. 3.22. n-MOSFET Threshold voltage evolution versus time during the BSI test. (a) For a non-irradiated sample and (b) for a 10 MeV 5·10^{13} cm^{-2} proton irradiated MOSFET

interface. ΔV_{TH} behaviour with time is shown in [Fig.3.23.b]. Despite of the weak ΔV_{TH} amplitude of the irradiated MOSFETs, we evidenced strong variations with the increase of time stress, especially for a proton fluence of 5·10^{13} cm^{-2}. This indicates a strong charge trapping and detrapping event. at the SiO_2/SiC interface occurring during a positive bias stress. Curiously, the event is less significant in the case of 5·10^{12} cm^{-2} and 5·10^{14} cm^{-2}. Nowadays, this peculiar behaviour is not fully understood. A possible explanation of the ΔV_{TH} increase could be the following. The faster the proton beam during irradiation, the less probability of atomic

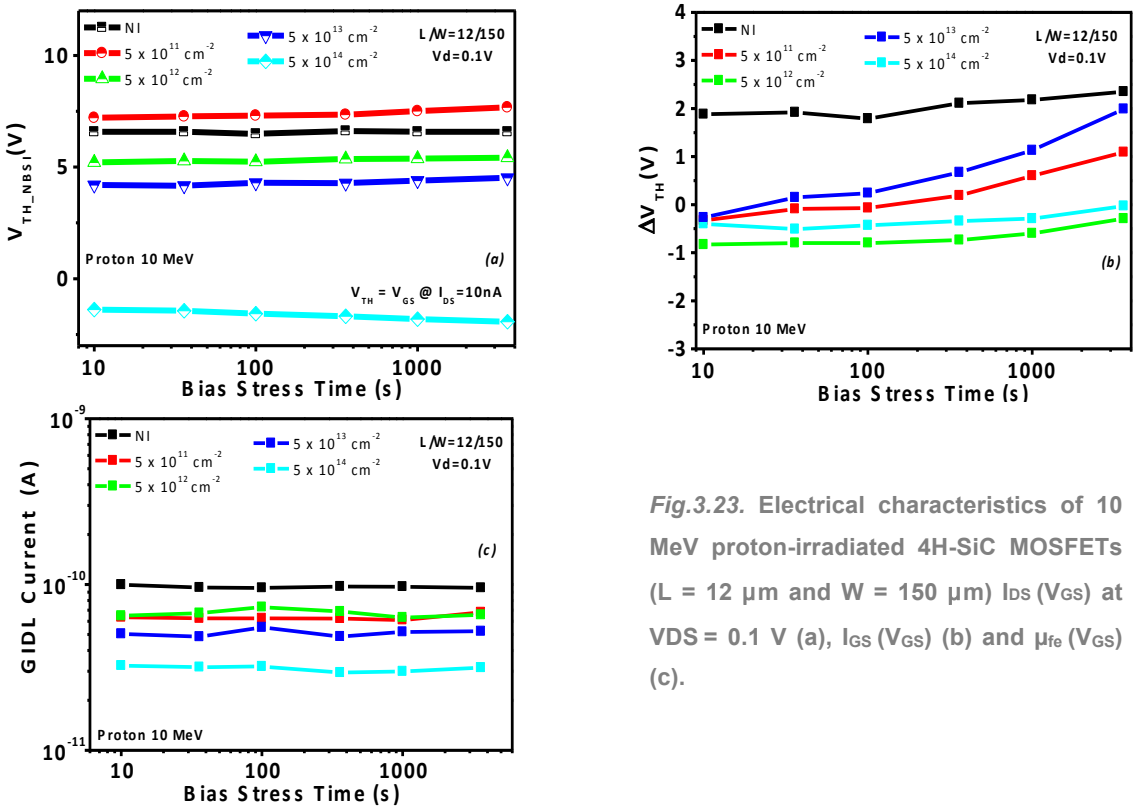


Fig.3.23. **Electrical characteristics of 10 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at VDS = 0.1 V (a), I_{GS} (V_{GS}) (b) and μ_{fe} (V_{GS}) (c).**

interaction with the MOSFETs. We suspect these damages generate a high quantity of free hole in the oxide that reach the SiO_2/SiC interface, and tunnel to the channel only after a positive gate bias and after a given stress time (because V_{TH_NBSI} is stable). This is in agreement with the fact that polaron transport is a slow phenomenon [5]. However, after irradiation, and despite the instability, the introduced interface trap and oxide charge trap during the stress has globally been decreased by a factor up to 7 (see Table 3.7) in comparison with the NI MOSFETs. However, if an impact occurs, the crystal lattice may be much more damaged with a high energy proton beam

Other electrical parameters

As seen in figure [Fig 3.23.c] no significant GIDL current is detected. Note that the measured GIDL current below 10^{-10} A is generally attributed to noise, since the equipment does not allow detecting such low current levels. As reported in Table 3.7, V_{BR_oxide} also slightly increased with irradiation, showing that, at room temperature, proton irradiation has no negative impact on the maximum voltage that the gate can stand. Concerning saturation current, in the case of the MOSFETs irradiated with fluences of $5\cdot10^{12}$ cm^{-2} and $5\cdot10^{13}$ cm^{-2} and despite that μ_{fe} is higher than the value before irradiation, $I_{D\_SAT\_MAX}$ presents lower values than those measured before irradiation. MOSFET sample irradiated at a fluence of $5\cdot10^{14}cm^{-2}$ has shown a drastic increase of the $I_{D\_SAT\_MAX}$ by more than 16 times in comparison with the NI MOSFETs. This increase is due to the drastic increase of μ_{fe} (8 times higher than in the NI case) together with the decrease of V_{TH}. This degradation, together with the V_{TH} and ΔV_{TH} stability issues could be corrected by an adapted annealing process. Still, the MOSFETs have shown a strong robustness to high irradiation energy. Due to the ΔV_{TH} good stability of the irradiated sample at a fluence of $5\cdot10^{14}cm^{-2}$, its lower V_{TH} and its higher μ_{fe}, the optimum fluence allowing a significant improvement of the MOSFETs EP should be slightly higher than $5\cdot10^{13}$ cm^{-2} in order to guarantee a positive threshold voltage value, a correct time stability and $I_{D\_SAT\_MAX}$ superior or equal to the one of the NI samples. Despite of the field effect mobility increase with high fluence, threshold voltage stability issues under BSI is stronger in high irradiation energies.

Electrical Parameters	Non Irradiated	Proton Energy: 10 MeV			
		$5\cdot10^{11}$ cm^{-2}	$5\cdot10^{12}$ cm^{-2}	$5\cdot10^{13}$ cm^{-2}	$5\cdot10^{14}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ [V]	6.58	7.21	5.21	4.24	-1.38
V_{oxide_br} [V]	23.42	31.1	27.5	26.1	27.2
$\mu_{fe\_Vg=12V}$ [$cm^2.V^{-1}s^{-1}$]	1.20	0.49	1.77	2.85	8.29
$I_{D\_SAT\_MAX}$ [µA]	15.33	2.52	11.35	10.67	241.1
$\lvert N_{it} + N_{ox} \times 10^{12}\rvert$[$cm^{-2}$]	1.06	0.18	0.22	0.15	0.47

Table 3.7. 4H-SiC n-MOSFET main electrical parameters before and after 10 MeV proton irradiations at four different fluences.

Time annealing impact

At the lowest irradiation fluence ($5\cdot10^{11}$ cm^{-2}), the annealing process has shown that, the longer the annealing time, the higher the $V_{TH:NBSI}$ [Fig 3.24.a], thus, the higher the predominance of acceptor traps with annealing time. For MOSFETs irradiated with fluences of $5\cdot10^{12}$ cm^{-2} and $5\cdot10^{13}$ cm^{-2}, the experimental V_{TH_NBSI} observed followed a curious trend [Fig 3.24.b and c]. With the increase of the annealing time, the V_{TH_NBSI} of the PIA MOSFETs starts to recover to the NI values before going back nearby their values after irradiation. These results are similar to those obtained in the case of the irradiated MOSFETs at 5 MeV and with a fluence of $5\cdot10^{14}$ cm^{-2}. This is very similar to Lelis et al. analysis: The defects removal may require much more time at 120°C to really obtain a "true annealing" where the trapped charge is totally removed. This experiment has shown a typical case where the oxide charges might be neutralized by the annealing, but the simple fact of applying an electric field can return the neutralized charges to its original state, thus not contributing to V_{TH_NBSI} recovery. In the case of the PIA MOSFETs irradiated at a fluence of $5\cdot10^{14}$ cm^{-2}, V_{TH_NBSI} is getting closer to its NI values with the annealing time increase [Fig 3.24.d] although the V_{TH} shift is relatively small. The evolution of ΔV_{TH} of the PIA MOSFETs irradiated at $5\cdot10^{11}$ cm^{-2} and $5\cdot10^{13}$ cm^{-2} didn't show any recovery effect, but a much better time stability than the one previously observed in the case of the irradiated MOSFETs [Fig 3.25.a and c]. This behavior is justified in section 3.4.6. Concerning the PIA of irradiated MOSFETs at $5\cdot10^{12}$ cm^{-2}, no change of the ΔV_{TH} stability have been observed [Fig 3,25.b]. The absence of recovery means that the annealing temperature was insufficient to induce any recovery. However, for a high irradiation fluence ($5\cdot10^{14}$ cm^{-2}), the ΔV_{TH} recovery with long annealing time occurred, donor charge traps start to be predominant during the BSI stress, giving an additional support to the statement that "true annealing" is slightly occurring in irradiated MOSFETs at high fluences [Fig 3.25.d]. As a consequence, an increase of the $|N_{ox}+N_{it}|$ brought by the BSI stress is observed [Table 3.8]. The extracted μ_{fe} of the PIA MOSFETs is in accordance with the V_{TH_NBSI} variation: It shows a decreasing tendency with annealing time at $5\cdot10^{11}$ cm^{-2} [Fig. 3.26.a], it didn't change at $5\cdot10^{12}$ [Fig. 3.26.b] and $5\cdot10^{13}$ cm^{-2} [Fig. 3.26.c], and shows a beginning of recovery tendency at $5\cdot10^{14}$ cm^{-2} [Fig. 3.26.d]. Furthermore, the subthreshold drain current average and the oxide breakdown voltage present

10 MeV Proton Fluence (p/cm^2)	**NI**	**$5\cdot10^{11}$**		**$5\cdot10^{12}$**		**$5\cdot10^{13}$**		**$5\cdot10^{14}$**	
		IRR	**ANN**	**IRR**	**ANN**	**IRR**	**ANN**	**IRR**	**ANN**
$V_{TH\_NBSI\_t=10s}$ (V)	6.58	7.21	11.2	5.21	5.13	4.24	4.71	-1.38	-0.77
V_{oxide_br} (V)	23.42	31.1	29.8	27.5	26.8	26.1	27.5	27.2	27.0
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	1.20	0.53	0.16	1.73	2.02	2.75	2.62	7.75	7.12
$I_{D\ SAT\ MAX}$ (µA)	15.04	2.49	1.70	11.26	12.09	10.60	9.33	236.01	239.4
$\lvert N_{ox} + N_{it}\rvert$ x 10^{12} cm^{-2}	1.06	0.18	0.05	0.22	0.26	0.15	0.25	0.47	0.51

Table 3.8. The extracted electrical parameters on irradiated at 10 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#1.

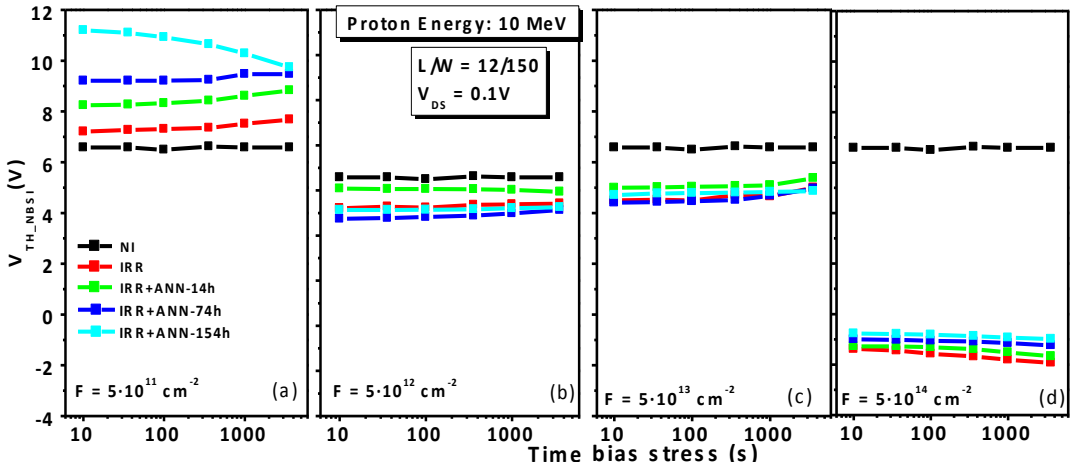


Fig 3.24. The threshold voltage time evolution after a NBS for 10 MeV proton irradiated MOSFETs#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

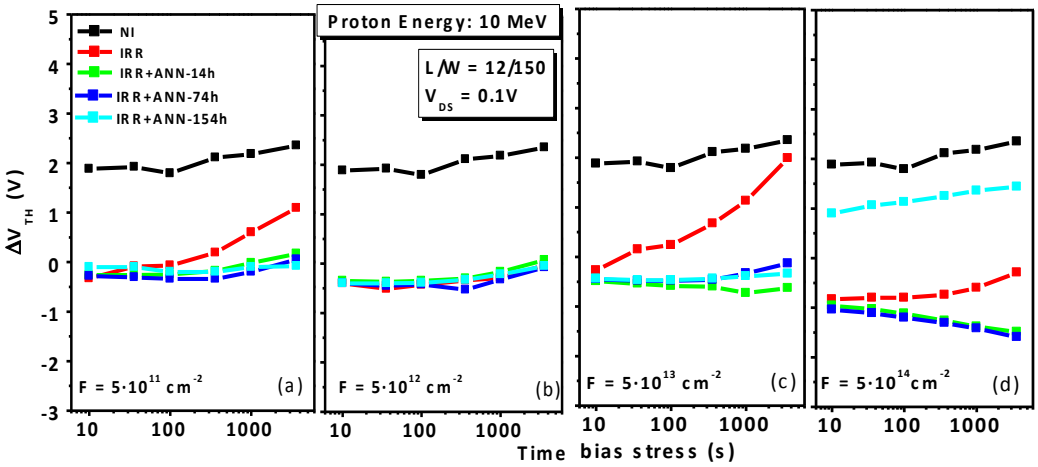


Fig 3.25. The threshold voltage hysteresis time evolution for 10 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d)) after irradiation and several time annealing (14h, 74h and 154h).

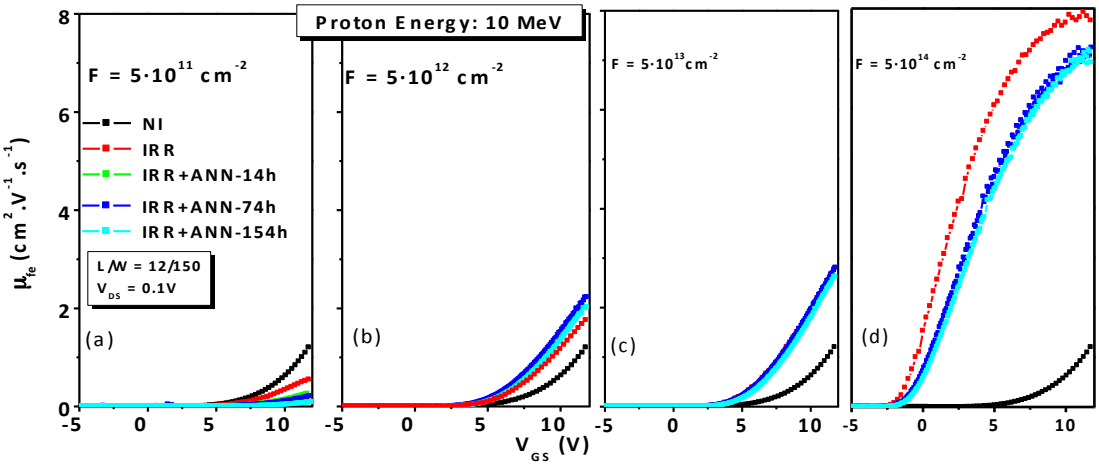


Fig 3.26. The field effect mobility time evolution after a NBS for 10 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

negligible changes, hence being mainly unaffected by both charged particles and by the post-annealing process. The main variation of EP is indexed in [Table 3.8]. Similarly to other cases, the V_{oxide_br} didn't show any variation after the PIA process.

3.4.4. Bias Temperature Instability Impact

The temperature experiment has allowed observing four types of behaviours not only on the PIA MOSFETs but also on the NI ones. The first one concerns V_{TH}, and the two others are related to μ_{fe}. Indeed, for all the irradiated and NI devices, an unexpected V_{TH} drift repeatedly occurs when increasing the temperature (see Fig. 3.27). Indeed, V_{TH} usually decreases, as it was shown in section 2.5. In these analysed cases, V_{TH} starts decreasing within the temperature r ange of [25ºC ; 100ºC]. In the temperature range of [100ºC ; 150ºC], V_{TH} remains

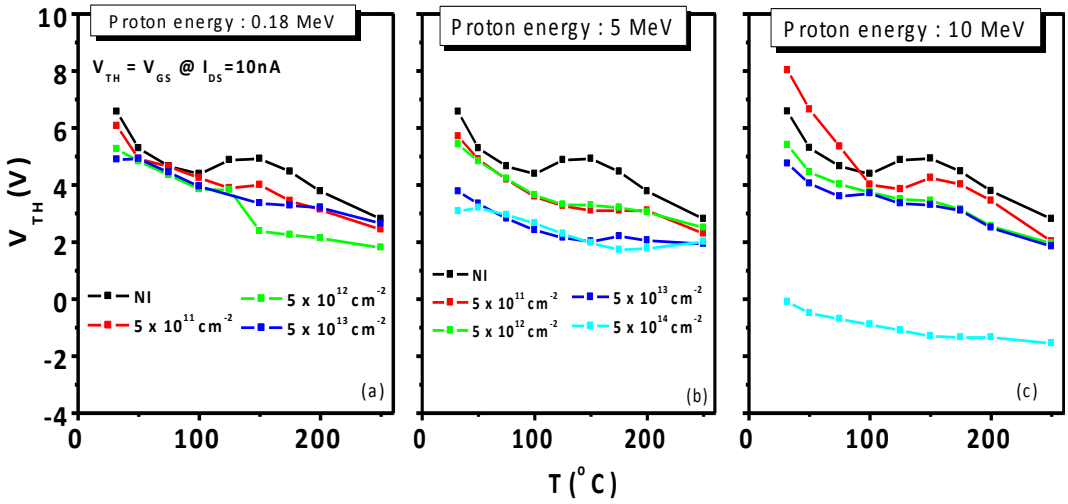


Fig 3.27. The V_{TH} temperature evolution for the NI MOSFETs and PIA MOSFETs of all fluences and fluences at a proton irradiation of 0.18 MeV (a), 5 MeV (b) and 10 MeV (c) proton irradiation respectively

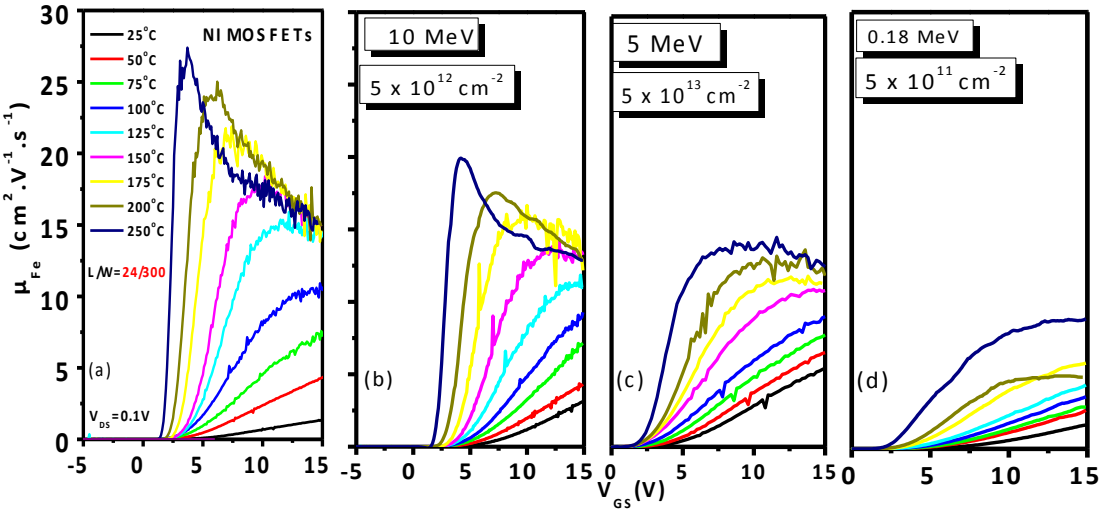


Fig 3.28. Evolution of the effective channel mobility with the increase of temperature for non-irradiated (a) and PIA MOSFETs irradiated at 10 MeV with a proton fluence of 5×10 ^{12} cm^{-2} (b), at 5 MeV with a proton fluence of 5×10^{13} cm^{-2} (c), and at 0.18 MeV with a proton fluence of 5×10^{11} cm^{-2} (d).

either constant, as it is the case of the PIA MOSFETs irradiated at 0.18 MeV [Fig 3.27.a] and 5 MeV [Fig 3.27.b], or increases, as it is the case of the NI MOSFETs, PIA MOSFETs irradiated at 10 MeV [Fig 3.27.c] with a fluence of $5 \cdot 10^{11} cm^{-2}$ and the PIA MOSFETs irradiated with electrons [Fig 3.27.d] . Above 150ºC, V_{TH} starts decreasing. The fact that the NI MOSFETs show the same behavior indicates that the V_{TH} turnover issue is not really related to the irradiation impact but to other issues detailed in section 3.4.6.

Similar μ_{fe} behavior to that of the NI MOSFETs [Fig 3.28.a] were founded on PIA MOSFETs proton irradiated at 10 MeV for all fluences. The experimental results for a fluence value of $5 \cdot 10^{12} cm^{-2}$ is shown in Fig 3.28.b that are acceptable, espescially when the gate bias is high (V_{GS} > 12V). In all the previous cases, neither the irradiation nor the long time annealing at 120ºC have impacted the μ_{fe} evolution with the gate to source voltage. At high temperature annealing, the roughness scattering is the predominant issue that determines μ_{fe} value, since it decreases when increasing the gate voltage. The last observation is the surface roughness increase on a large number of PIA MOSFETs irradiated at 5 MeV and 0.18 MeV [Fig 3.28.c and d], preventing the μ_{fe} increase at low gate voltages and leading to its direct saturation, even at the highest temperature. Indeed, due to the damage generated by irradiation at the vicinity of the SiO_2/SiC interface, the MOSFET surface roughness is getting so critical that it even predominates over the coulomb and phonon scattering mechanisms. As a consequence, no μ_{fe} peak is observed. In addition, the lower the irradiation energy, the lower the maximum μ_{fe} reached at high temperature. These results confirm that low irradiation energies have a negative impact on μ_{fe}, which is more relevant at low gate voltages. Furthermore, the gate leakage current of all the irradiated and post-annealed MOSFETs is not relevant and similar to the NI samples, remaining below 2 nA at 250ºC.

3.4.5 Understanding of the MOSFET increase of effective channel mobility

At the SiO_2/SiC interface of an oxynitrided gate oxide MOSFET, complexes such as SiO_xN_y or $O_xN_yC_z$ exist [51]. When the irradiation beam crosses the MOSFETs [Fig 3.29.a], the passivated bonds are broken during irradiation (N and H in minor extend) [Fig 3.29.b], and e-h pairs are created [Fig 3.29.c]. Indeed, in [52] it has been reported that O-Si-N complex exists in the crystalline lattice after performing a similar oxidation process [53]. Additionally, it has been shown that the O-Si-N complexes are efficient electron trap centres [54]. Therefore, when a neutral O-Si-N molecule close to the SiO_2/SiC interface is electrically activated, a negative SiO^- charge is created at the SiO_2/SiC interface. This N-depassivation reaction can be described with the following diffusion-limited electrochemical reaction [54]:

$$O\text{-}Si\text{-}N + e^- \leftrightarrow O\text{-}Si^{\bullet} + N^{\circ} \qquad (3.3)$$

The charged N atoms are bonded to some other Si atoms in the SiO_xN_y transition layer. It is indeed feasible that the negative charge is localized on a Si atom after the electron is captured by the N atom, weakening the corresponding Si-N bond [55], hence making the N atoms more susceptible to diffuse than the other species [Fig 3.29.d]. Moreover, at the SiO_2/SiC

interface, a large number of oxide vacancies exist due to the out-diffusion of O into the oxide layer [56], acting as trapping centers. The proton irradiation damage inside the p-type epilayer and in the n-substrate generates eventually additional free e-h pairs that can be trapped at the SiO_2/SiC interface [Fig 3.29.e]. Furthermore, we have assumed that the N atoms and, in a minor extend, the residual H atoms, which are currently located at the SiO_2/SiC interface, are forced due to collisions to diffuse deeper towards the epilayer during ion irradiation. Therefore, new bonds between H and N with Si and C could be created, leading to passivation improvement [Fig 3.29.f], and explaining the absence of C clusters and/or C containing by-products observed in [57]. Moreover, by breaking bond between Si and O, irradiation could induce an extra diffusion of the O atoms. As a result, a sub-oxide is expected to be formed [Fig 3.29.f] and hence the SiO_2/SiC interface gets more passivated [57-59]. The enhanced passivation may justify the MOSFETs oxide breakdown voltage increase after the irradiation process. Due to the irradiation process, the probability of having fixed charges and near interface charges due to dangling bonds may also slightly decrease due to N and H deeper passivation efficiency predominance over the charge accumulation during NBSI or PBSI and, therefore, raise the MOSFETs μ_{fe} and its time stability. Additionally, a second hypothesis can be established in the case of low proton energies up to 0.5 MeV which correspond to the theoretical proton irradiation energy limit before it penetrates into the n-type SiC substrate. In this case, the proton stops in the p-type epilayer or near the SiO_2/SiC interface, releases its energy and remains immobile. The release of energy can provoke small atomic displacement and can eventually damage the epilayer. However, when a positive gate bias is applied, the accumulation of electron at the epilayer surface can interact with the immobile proton and turn this proton into H atom. This way, the H atom can be connected to a nearby Si/C site. In the case of a connection with a C site, it contributes to enhance the C layer passivation.

In the previously presented experiments, the μ_{fe} generally increases when V_{TH} decreases, accounting for a predominance of N-diffusion together with a donor trap generation at the SiO_2/SiC interface. In the case of a μ_{fe} and V_{TH} decrease, the tunneling effect of the charges located at the epilayer, together with the epilayer damage by generation and displacement predominates. Moreover, the N-diffusion is assumed to be a function of the irradiation energy: The faster the particle beam, the deeper and the more efficient the N-diffusion, but the more important the damage in the epilayer and in substrate.

Finally, it is suspected that, if a high quantity of ionization particles of enough energy penetrates the P-well or the substrate, the damage area can be more important in the P-well than in the interface region. References [60] and [61] report that the DLTS experiment performed on irradiated 4H-SiC layer and diodes at low proton or electron energies (> 600 keV) could attribute these effects to the presence of Z1/Z2, EH4 EH5, EH6/7 trap centres. Therefore, it is assumed that for higher proton fluences or electron doses, the ionization effects could become more notable, hence degrading the device EP. However, for the studied doses, we believe that the N-diffusion process is predominant over the deep level defect generation due to the observed improvement of device's main EP, showing the irradiation importance in improving the robustness of oxinitrided gate oxide MOSFETs.

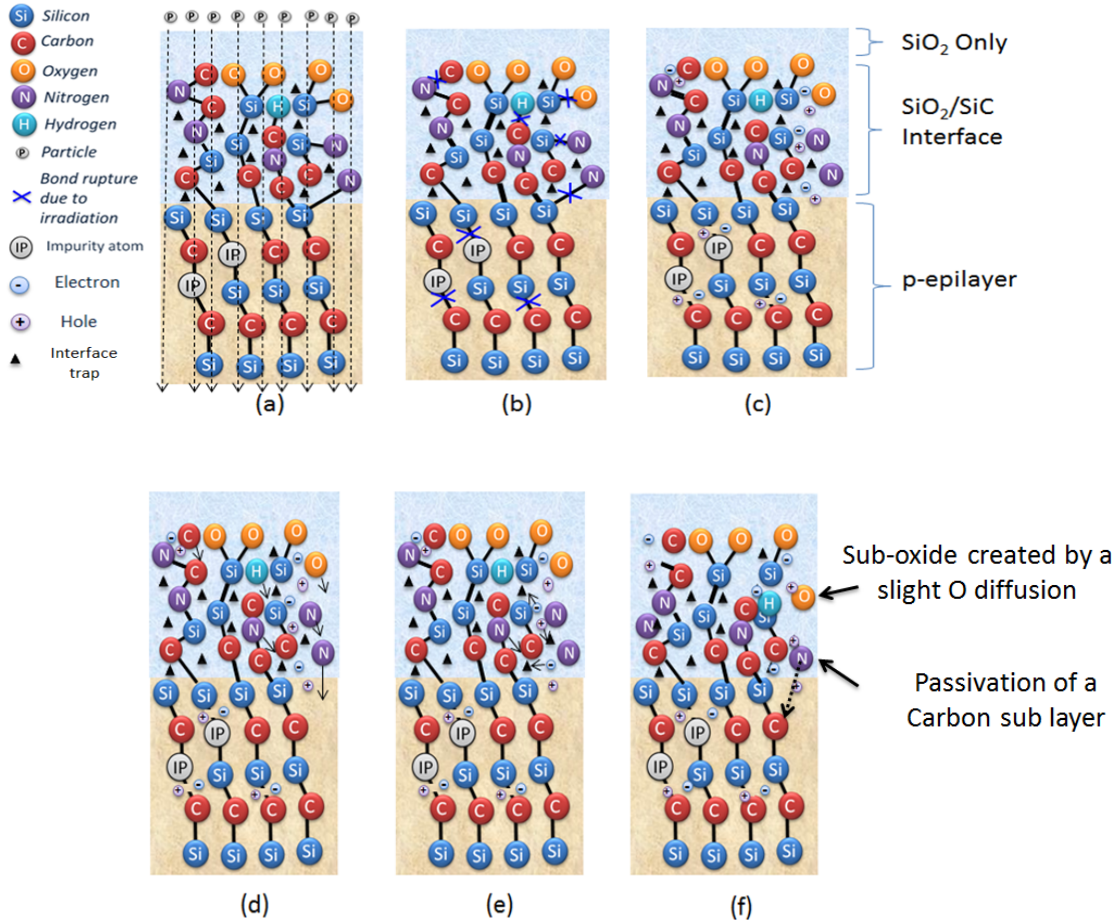


Fig.3.29. SiO_2/SiC interface MOSFETs: Small diffusion mechanism theory of the passivated species that allow an increase of the μ_{fe} and V_{oxide_br}. The particle beam crosses the SiO_2/SiC interface and epilayer (a), breaking several bonds between atoms (b), generating electron hole pair (c). It will induce a small diffusion of the passivated species and the oxygen atoms (d). Some of the generated e-h pairs will either fall into an interface trap or introduce allowed level in the semiconductor bandgap (e). By diffusing, N and H atoms will passivate a sublayer of carbon atom meanwhile o will create a very thin sub-oxide layer (f).

3.4.6 Recovery mechanism at the SiO_2/SiC interface

As predicted in the Si case [62-64] a recovery of the main electrical parameter was expected along annealing time at a specific temperature (in our case 120ºC). However, in the case of PIA 4H-SiC MOSFETs, we have observed a different behaviour from Si MOSFETs. Indeed, due the presence of nitrogen in the gate dielectric layer, the classic recovering model established for Si MOSFET [16] is accurate but limited. It is believed that during the annealing, several phenomena may take place, including the e-h pairs recombination already discussed in section 3.2. Let focus on the initial situation at the SiO_2/SiC interface and the p-epilayer before the irradiation occurred [Fig 3.30.a]. The irradiation process at the transition layer is fully described in the previous sections 3.3.1 and 3.4.5. At the end of the irradiation process [see fig 3.29.f], we have suggested that dangling bond are created in the transition layer and, in very

minor extend, in the 4H-SiC epilayer [Fig 3.30.b]. Then, fives phenomena can be taken into account during the annealing. They may all occurs at the same time:

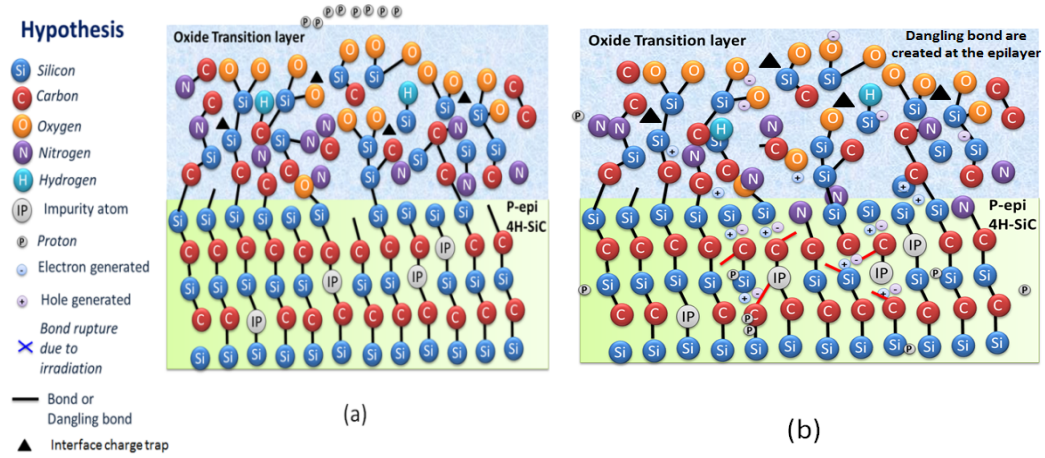
1) Extra Nitrogen diffusion, as previously mentioned in the previous section. Indeed, it is believed that both time and temperature annealing can contribute to very slightly move the nitrogen atoms, contributing to an additional passivation and might justify why, if this phenomenon is predominant, a μ_{fe} increase is observed while keeping the V_{TH} time stability constant. Additionally, the e-h recombination occurs as well, and is represented in [Fig 3.30.c]. If this phenomenon is predominant over the others, the recovery of the electrical parameter is observed.

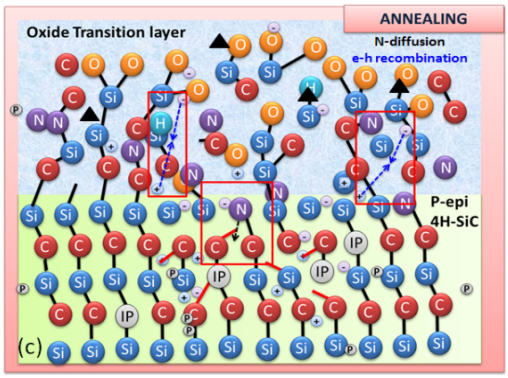
2) Tunneling to the oxide layer of ion charges generated by irradiation and located in the epitaxial layer at the vicinity of the SiO_xN_y transition layer [Fig 3.30.d]. Once tunneled, charges can either recombine inside the transition layer (the recovery is observed) or trapped at interface traps (V_{TH} shift depending on the charge nature).

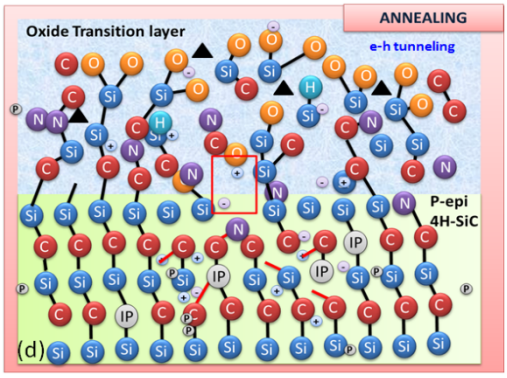
3) The generated charges can be trapped by the oxide charge traps moving inside the oxide layer during the annealing [Fig 3.30.e], and provokes a V_{TH} instability with BSI. On the contrary, if a charge has already been trapped inside the oxide before the annealing process, the annealing temperature might be high enough for the trapped charge to get out of the trap and behave like a free carrier. It will contribute in that case to the creation of additional interface charges.

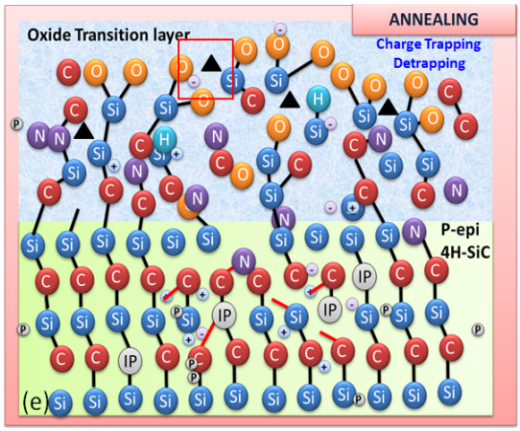
4) A very small quantity of hydrogen atoms can be created by electron charge trapping of the remaining protons inside the epilayer [Fig 3.30.f and g]. If this effect predominates, a V_{TH} instability might be observed during the BSI stress [65]. Thus, in the case of low proton irradiation energy, it is very complex to attribute the observed V_{TH} instability to a specific effect.

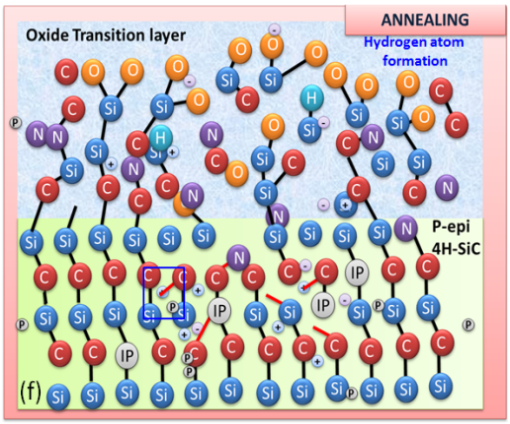
As far as the temperature annealing process is concerned, an important issue has been detected: How does the temperature increase can induce a V_{TH} turnover in some cases and why, in others, this turnover does not occur, but remain constant? We suggest that it can be due to either the huge amount of screw edge dislocation density [66-67] that might start playing a role at temperatures above 100ºC, or to charge trapping at deep energetic levels inside the 4H-SiC bandgap [68], meaning that a high temperature is required to activate these deep level traps. In fact, irradiation creates deep level traps within the epilayer [60]. If the deep traps have an acceptor nature and are activated at high temperatures, they could prevent the V_{TH} decrease with temperature. When the temperature is very high, these defects do not act anymore, and the roughness scattering clearly predominates. Therefore, V_{TH} keeps on decreasing. This temperature effect only occurred on epitaxied 4H-SiC MOSFETs. Indeed, the same irradiation and temperature experiments have been already performed on implanted 4H-SiC MOSFETs (chapter 6), and V_{TH} monolithically decreases when increasing temperature.











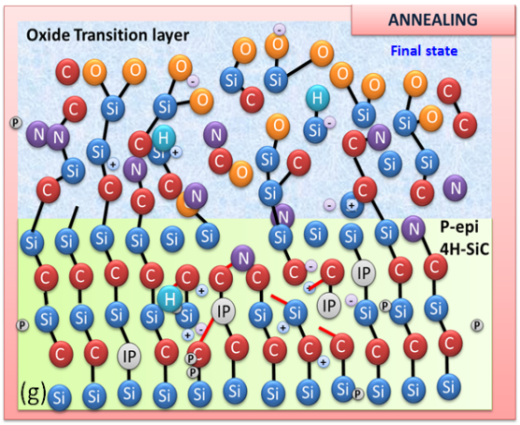


Fig.3.30. The annealing recovery mechanism steps at the epilayer and at the SiO_2/SiC interface. Including the initial situation (a), the situation after irradiation (b), the N-diffusion and e-h recombination (c), the e-h tunnelling (d), the charge trapping and detrapping (f), and the hydrogen atom creation (e) leading to the final state (g)

3.4.7. Conclusion on irradiated MOSFETs having a N_2O gate oxide

Globally, the irradiation process of 4H-SiC MOSFET having an oxinitrided gate oxide is mainly dominated by two main factors. The first one is the trap generation and charge build-up mechanism that occurs during irradiation. This is a different mechanism from that of the Si-MOSFETs, since the interface traps have to be taken into account in order to explain the V_{TH} shift behaviour. The second one is the role of O, N and H atoms during the irradiation. The N diffusion at the SiO_2/SiC together with the H generation in the epilayer (for low irradiation energies) enhanced the C passivation, and provokes an increase of μ_{fe} and V_{br_oxide}. At a given irradiation energy, the predominance of one of the mentioned effects depends on the absorbed fluence/dose. Under all the irradiation conditions, the off-state drain and gate leakage currents show negligible variations accounting for no critical damage of the irradiated epilayer, and demonstrating that an oxinitrided gate oxide MOSFETs can be a viable solution for irradiation harshness. Finally, if the dose and irradiation energy is carefully chosen, the V_{TH} and ΔV_{TH} time stability can even be improved.

In addition, the post irradiation annealed behaviour of 4H-SiC MOSFET having a N_2O oxinitrided gate layers has been investigated by using the BSI technique. By submitting the irradiated MOSFETs to a post-annealing process, if the balance between the fluence and the oxide thickness is adequate, the mentioned electrical parameters experiment an additional improvement after annealing. The results obtained on the post-annealed SiC-MOSFETs are quite different from the recovery predicted for Si-MOSFETs. We believe that the nitrogen diffusion and the mobile ion charge tunneling from the epitaxial layer to the SiO_2 layer should be taken into consideration besides the typical electron-hole recombination. No gate leakage or GIDL current or impact on PIA process on oxide breakdown voltage has been shown. Thus, a specific conclusion for each irradiation energy case can be drafted.

Irradiated MOSFET#1 with a low proton irradiation energy: When increasing the fluence up to $5{\cdot}10^{12}$ cm^{-2}, V_{TH} decreases, reaching a minimum value at $5{\cdot}10^{12}$ cm^{-2}, while μ_{fe} and $I_{D\_SAT\_MAX}$ increases and reach their maximum values for $5{\cdot}10^{12}$ cm^{-2} as well. The μ_{fe} is five times higher and $I_{D\_SAT\_MAX}$ doubles with respect to their corresponding values of NI devices. However, at a higher fluence ($5{\cdot}10^{13}$ cm^{-2}), V_{TH} and μ_{fe} recover to their initial values due to the generated acceptor traps at the SiO_2/SiC interface that start to predominate. A low hysteresis associated with a high V_{TH} stability with BSI pulse duration is also observed. The optimum irradiation fluence has been founded to be $5{\cdot}10^{12}$ cm^{-2}.

PIA Process : In the best case, (F= $5{\cdot}10^{12}$ cm^{-2}), the long time annealing impact induced a small V_{TH} recovery with a small μ_{fe} increase, and induced an improvement of the ΔV_{TH} stability. In the worst case, (F = $5{\cdot}10^{11}$ cm^{-2}), the annealing induces a strong ΔV_{TH} instability. At high temperatures, an increase of the roughness scattering has been observed limiting the μ_{fe} value. Its maximum value at high gate voltages and high temperatures is 30% lower than in the NI

case. Thus, MOSFETs having an N_2O gate oxide irradiated at low energy has shown a better robustness of the EP at a proton irradiation of $5 \cdot 10^{12}$ cm^{-2}.

Irradiated MOSFET#1 with a medium proton irradiation energy: The higher the proton fluence, the higher the μ_{fe} value and the lower $V_{TH.}$ Moreover, ΔV_{TH} amplitude has been reduced with respect to NI devices. The maximum μ_{fe} is reached at irradiation fluence of $5 \cdot 10^{14}$ cm^{-2} and is more than 4 four times higher to the one of the NI samples. In comparison with the NI devices, $I_{D\_SAT\_MAX}$ doubles and the V_{TH} stability is improved, the ΔV_{TH} amplitude been reduced. However it seems that irradiation at a proton fluence of $5 \cdot 10^{14}$ cm^{-2} is too high to allow a correct long time stability. Thus, an optimum irradiation process allowing an EP improvement should be between $5 \cdot 10^{13}$ cm^{-2} and $5 \cdot 10^{14}$ cm^{-2}.

PIA Process: Long time PIA generally improved the ΔV_{TH} time stability without really provoking any recovery of the V_{TH_NBSI}. In one case ($F=5 \cdot 10^{13}$ cm^{-2}), it shows that PIA allowed the μ_{fe} MOSFET to increase before recovering. This fact puts in evidence the charge trapping/detrapping effect in addition with a possible and small N-diffusion occurring during the PIA process. μ_{fe} of PIA MOSFETs at high temperatures at $V_{gs} > 12V$ has shown similar values as that of NI MOSFETs, with an increase of the roughness scattering (but lower than in the case of 0.18 MeV). The MOSFETs having N_2O Gate oxide irradiated at medium energy has shown a better robustness of the EP at a proton irradiation fluence of $F = 5 \cdot 10^{13}$ cm^{-2}.

Irradiated MOSFET#1 with a high proton irradiation energy: The results have shown an EP MOSFET improvement. Among them, we have observed a μ_{fe} increase at irradiation fluences > $5 \cdot 10^{11}$ cm^{-2}. Moreover, the ΔV_{TH} presents a good stability with bias duration, firstly eliminating the large hysteresis between positive and negative stress, and secondly decreasing and then maintaining its value constant with time. However, this stability has been obtained with an irradiation fluence of $5 \cdot 10^{13}$ cm^{-2} (fluence giving the best EP results). A good V_{TH} time stability has also been obtained after an irradiation with fluence of $5 \cdot 10^{11}$ cm^{-2}, the V_{TH_NBSI} increased and the μ_{fe} decreased with respect to the NI samples. Thus, high irradiation energy could be an acceptable process for improving the electrical parameter and correcting the issues related to threshold voltage instability. However, a trade-off between fluence/V_{TH} stability/increase of μ_{fe} has to be founded.

PIA Process: The results clearly allowed putting in evidence the PIA impact on the ΔV_{TH} stabilization. It also shows that a low irradiation fluence can induce an important V_{TH} positive shift with annealing time, and, on the other hand, very high irradiation fluence can induce small EP recovery. The remarkable point is that no matter the irradiation fluence, high temperature annealing does not affect μ_{fe} at $V_{GS} > 12V$. The MOSFETs having N_2O Gate oxide irradiated at high energy has shown a better robustness of the EP at a proton irradiation fluence between $5 \cdot 10^{13}$ and $5 \cdot 10^{14}$ cm^{-2}.

3.5. Proton irradiation of MOSFETs with N_2O + TEOS Gate oxide

The study of irradiation impact on MOSFET#1 with a poor SiO_2/SiC interface quality has been carried out in the previous section. Now, the evaluation of the irradiation impact will be carried out on MOSFET having a better quality of gate oxide (MOSFETs#2). To improve this quality, hydrogenation at 800ºC has been used for surface cleaning (instead of 900ºC in the case of the fabricated MOSFET#1). A thinner N_2O layer has been grown and a deposition of TEOS has been carried out after the oxinitridation as indicated in section 3.3.2.2.

3.5.1. Low-Energy proton Irradiated MOSFETs

Effect of radiation fluence on the transconductance

Although the effective oxide thickness for N_2O+TEOS (82 nm) MOSFETs#2 is higher than N_2O gate oxide (38 nm) MOSFETs#1, V_{TH} for MOSFETs#1 is slightly lower than MOSFETs#2 [see Fig 3.31.a and Fig 3.9.a]. This is due to a higher bulk oxide charges density introduced by the TEOS deposition layer. The gate leakage current didn't show any variation for all irradiated MOSFETs [Fig 3.31.b]. The extracted μ_{fe}, and I_{DSAT_MAX} before irradiation present higher values than those of the N_2O gate oxide MOSFETs#1, as shown in [Fig 3.31.c] and [Fig 3.31.d], respectively. Despite these improvements, the MOSFETs quality before irradiation remained limited in the sense that μ_{fe} is still way below the values founded in the literature

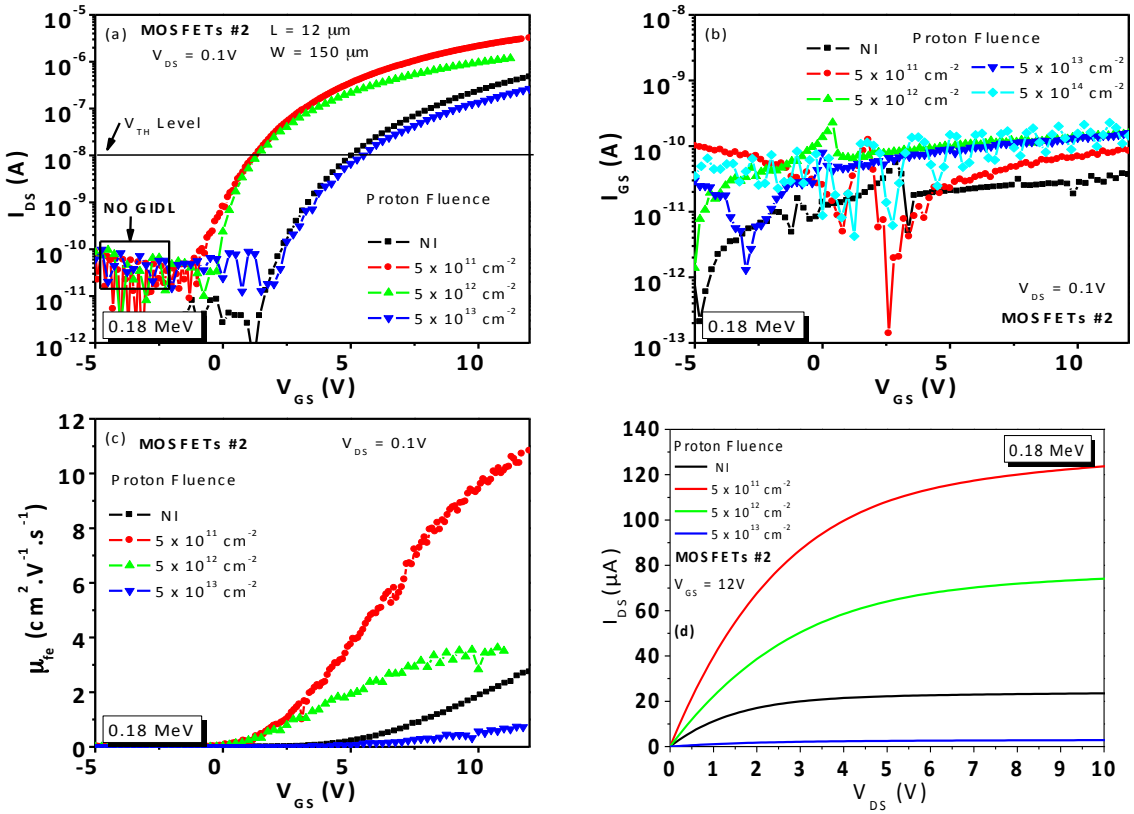


Fig 3.31. **Electrical characteristics of 0.18 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b), μ_{fe} (V_{GS}) (c) and I_{DS} (V_{DS}) at V_{GS} = 12V.**

[69-71]. The I_{DS} (V_{GS}) curves have evidenced the existence of "a threshold fluence" (F_{TH}) that change the interface trap predominance at the SiO_2/SiC interface from donor to acceptor, as it was the case in MOSFETs#1. Any change in the direction of the V_{TH} drift has been obtained since no experiments have been carried out at fluences lower than $5{\cdot}10^{11}$ cm^{-2}, $F_{TH} \cong 5{\cdot}10^{11}$ cm^{-2}. Experimental results show that for F_{TH} values than $5{\cdot}10^{11}$ cm^{-2}, the amount of prevailing trap donors at the interface starts to decrease compared to trap acceptors. For the highest fluence ($5{\cdot}10^{13}$ cm^{-2}), the interface trap acceptor number clearly start to predominate at the SiO_2/SiC interface due to the positive shift of the I_{DS}(V_{GS}) curves comparing to that of the NI MOSFETs. μ_{fe} shows a very strong increase after irradiation (more than 4 times than NI samples) but this increase is observed at a fluence of $5{\cdot}10^{11}$ cm^{-2}. In section 3.4.1, the same μ_{fe} increase was observed when comparing the irradiated MOSFETs to the NI ones at $5{\cdot}10^{12}$ cm^{-2} proton fluence for a similar irradiation energy. Moreover, μ_{fe} at V_{GS}=12V and for the mentioned fluence is higher in the N_2O gate oxide MOSFETs. In accordance with the μ_{fe} increase, the maximum saturation current increases with the irradiation fluence before collapsing when fluence is higher than $5{\cdot}10^{12}$ cm^{-2}.

BSI stress

BSI measurements revealed an improved V_{TH_NBSI} time stability of the irradiated samples, in comparison with the NI ones [Fig 3.32.a]. Nevertheless, the results obtained also reveal that the V_{TH_NBSI} stability of the NI **MOSFETs #2** is worse than NI **MOSFETs #1** [Fig 3.10.a]. However,this instability is corrected by the proton irradiation, no matter the absorbed fluence [Fig 3.32.a]. The GIDL current, although not shown, presents average values similar to that shown in section 3.4 (GIDL < 10^{-10} A). The amount of generated interface and oxide traps with time stress is calculated from the ΔV_{TH} characteristic through equation (eq 2.15) and its value after the first stress is reported in [table 3.7] as in the other previous sections. ΔV_{TH} time instabilities of irradiated MOSFET with fluences of $5{\cdot}10^{11}cm^{-2}$ and $5{\cdot}10^{12}$ cm^{-2}, slightly improved with respect to the NI MOSFETs [Fig 3.32.b], but after 1000 s of BS, ΔV_{TH} starts following a

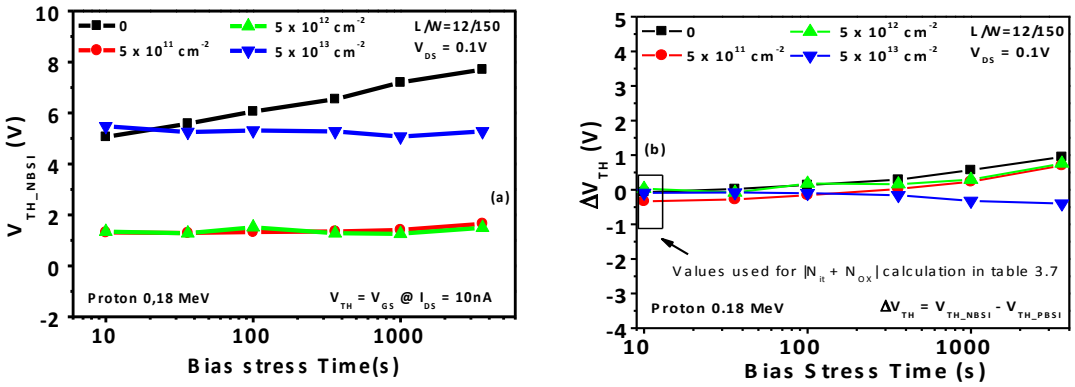


Fig 3.32. **Electrical characteristics of 0.18 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) V_{TH_NBSI} = f (t) at V_{ds} = 0.1 V (a), and ΔV_{TH} = f(t) (b).**

similar tendency as the NI MOSFETs. In addition, almost no hysteresis has been detected in the case of MOSFETs irradiated at $5 \cdot 10^{13}$ cm^{-2} after 1h stress, and an important time stability improvement has been observed.

Other Parameters

For the irradiated MOSFETs#2 at a fluence of $5 \cdot 10^{13}$ cm^{-2}, a decrease of the oxide breakdown voltage has been observed (Table 3.9) when compared to the NI MOSFETs#2. This behaviour is similar to that observed for MOSFETs#1 at low energy proton irradiation but in this case the oxide breakdown voltage decrease is more noticeable. This is related to the fact that more e-h pairs are generated in the oxide since the thicker oxide of MOSFETs#2. At low irradiation energy and when the fluence overcomes $5 \cdot 10^{12}$ cm^{-2}, the e-h pair generated effect seems to predominates over the other phenomena. The summary of the main EP variation is represented in Table 3.9. When compared with the NI MOSFETs, the irradiated MOSFET at the lowest fluence has shown the most important EP improvement. However F_{TH} is lower than F_{TH} observed in 3.3.1 ($F_{TH} = 5 \cdot 10^{12}$ cm^{-2} in 3.3.1 and $F_{TH} = 5 \cdot 10^{11}$ cm^{-2} in this section) because of the thicker oxide: the fluence threshold is reduced since threshold voltage shift is not only determined by the interface trap predominance at the SiO_2/SiC interface from donor to acceptor but also by the positive charge excess due to hole accumulation near the SiO_2/SiC interface.

Electrical Parameters	Non Irradiated	Proton Energy: 0.18 MeV		
		$5 \cdot 10^{11}$ cm^{-2}	$5 \cdot 10^{12}$ cm^{-2}	$5 \cdot 10^{13}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ (V)	5.06	1.31	1.34	5.48
V_{oxide_br} (V)	47.20	47.50	50.10	31.20
$\mu_{fe\_Vg=12V}$ ($cm^{-2}.V^{-1}s^{-1}$)	2.70	12.30	3.44	2.32
$I_{D\_SAT\_MAX}$ (µA)	23.23	123.1	74.4	3.07
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert [cm^{-2}]$	0.040	0.190	0.017	0.013

Table 3.9. 4H-SiC n-MOSFET main electrical parameters before and after a 0.18 MeV proton irradiations at three different fluences.

Time annealing impact

PIA MOSFETs#2 irradiated at a fluence of $5{\cdot}10^{11}$ cm^{-2} show a clear recovery tendency of the V_{TH_NBSI} [Fig 3.33.a], although for fluences of $5{\cdot}10^{12}$ cm^{-2} and $5{\cdot}10^{13}$ cm^{-2} the annealing effect is opposite to the expected recovery effect: The V_{TH_NBSI} decreases in comparison with the irradiated MOSFETs [Fig 3.33.b and c]. The ΔV_{TH} instability issues noted in the case of PIA MOSFETs#1 irradiated at 0.18 MeV, do not occur at $5{\cdot}10^{11}$ cm^{-2} [Fig 3.34.a], but it happens at $5{\cdot}10^{12}$ cm^{-2} [Fig 3.34.b]. This mean that at this fluence, a surplus of donor traps acts at the SiO_2/SiC interface during the BSI stress. The value of effective $|N_{ox} + N_{it}|$ that entered at stake during the last BSI stress (t=3600s) has been founded to be around $1.1{\cdot}10^{12}$ cm^{-2}, whereas in the case of the NI MOSFETs, this value is about $5.4{\cdot}10^{11}cm^{-2}$. This phenomenon is not fully understood due to the fact that no ΔV_{TH} instability has been observed with the increase of the fluence for both MOSFETs#1 and MOSFETs#2. At F = $5{\cdot}10^{13}$ cm^{-2}, no real variation of ΔV_{TH} has been observed [Fig 3.34.c]. The μ_{fe} of PIA MOSFETs#2 irradiated at F = $5{\cdot}10^{11}$ cm^{-2} also seems to start recovering [Fig 3.35.a] together with the V_{TH_NBSI} values. However, μ_{fe} values remain much higher than the NI samples. At F = $5{\cdot}10^{12}$ cm^{-2}, and with the decrease of V_{TH}, μ_{fe} increases drastically with annealing time in comparison with the irradiated MOSFET [Fig 3.35.b]. The reason of such an increase has been given in the first case of the section 3.4.6. At F = $5{\cdot}10^{13}$ cm^{-2}, μ_{fe} is almost completely recovered [Fig 3.35.c], although it has relatively low values due to the lattice damage. According to Table 3.10, the oxide breakdown voltage didn't show any change of their values in comparison with the one before the PIA process. The long annealing time didn't help the MOSFETs#2 irradiated at $5{\cdot}10^{13}$ cm^{-2} oxide breakdown voltage torecover to its non-irradiated values. It is reminded that, the term $|N_{ox} + N_{it}|$ is extracted after the first cycle of BSI stress (t=10s). The variation of this parameter in not considered as very important due to the fact that a ΔV_{TH} variation of 0.18V correspond to an $|N_{ox} + N_{it}|$ variation of 10^{11} cm^{-2}.

0.18 MeV Proton Fluence (cm^{-2})	**NI***	**$5{\cdot}10^{11}$**		**$5{\cdot}10^{12}$**		**$5{\cdot}10^{13}$**	
		IRR*	**ANN***	**IRR**	**ANN**	**IRR**	**ANN**
$V_{TH\_NBSI\_t=10s}$ (V)	5.06	1.3	2.17	1.3	0.45	5.5	5.48
V_{oxide_br} (V)	47.1	47.1	47.2	50.0	49.8	31.2	31.0
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	2.74	12.7	10.56	3.4	10.56	0.67	2.48
$I_{D\_SAT\_MAX}$ (µA)	23.7	123.6	63.7	74.5	112.1	2.5	18.6
$\|N_{ox} + N_{it}\|$ x 10^{12} cm^{-2}	0.040	0.190	0.25	0.017	0.17	0.013	0.05

Table 3.10. The extracted electrical parameters on irradiated at 0.18 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#2. NI= MOSFETs measured prior to irradiation, IRR = MOSFETs measured after irradiation and ANN = MOSFETs measured after 154h of post irradiation annealing.

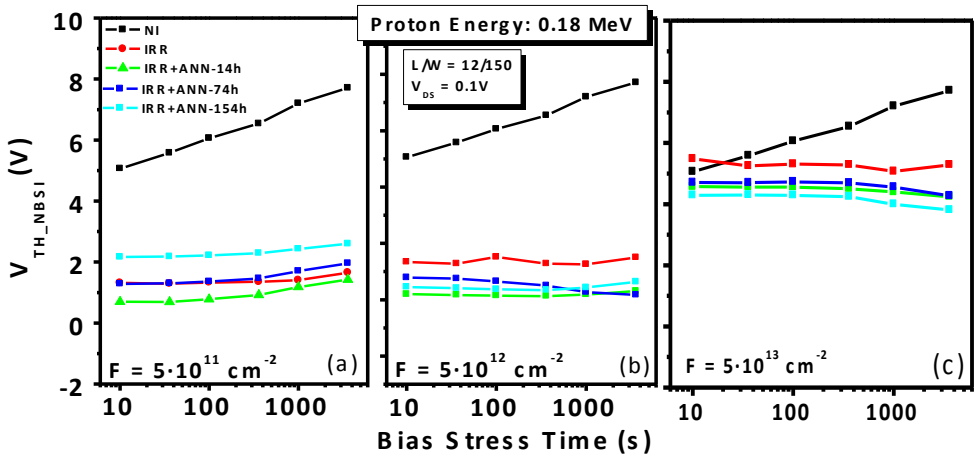


Fig 3.33. The threshold voltage time evolution after a NBS for 180 keV proton irradiated MOSFETS#2 at $5\cdot10^{11}cm^{-2}$ (a), $5\cdot10^{12}cm^{-2}$ (b) and $5\cdot10^{13}cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

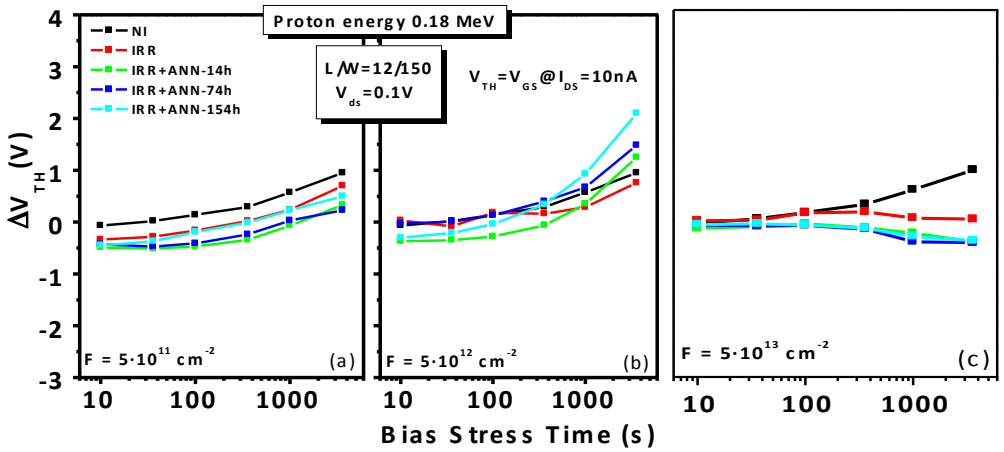


Fig 3.34. ΔV_{TH} time evolution for 180 keV proton irradiated MOSFETS#2 at $5\cdot10^{11}cm^{-2}$ (a), $5\cdot10^{12}cm^{-2}$ (b) and $5\cdot10^{13}cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

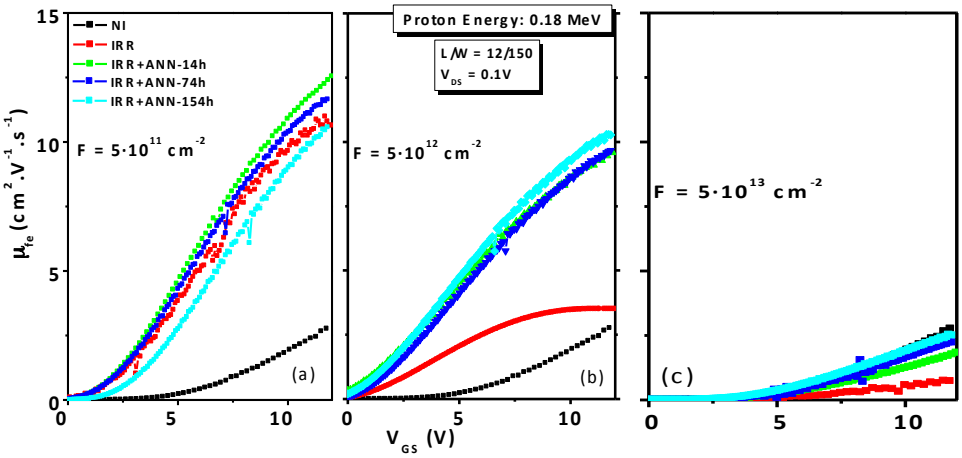


Fig 3.35. The field effect mobility time evolution after a NBS for 180 keV proton irradiated MOSFETS#2 at $5\cdot10^{11}cm^{-2}$ (a), $5\cdot10^{12}cm^{-2}$ (b) and $5\cdot10^{13}cm^{-2}$ (c) after irradiation and several time annealing (14h, 74h and 154h).

3.5.2. Medium-Energy proton irradiated MOSFETs

Effect of radiation fluence on the transconductance

The adopted MOSFETs electrical behaviour after a 5 MeV irradiation is similar to the one reported in section 3.4.2. However, the shift of the transconductance characteristic with the increase of the irradiation fluence is much higher than the one observed in the irradiated MOSFETs having a dielectric layer made with N_2O. Once again, the oxide thickness problematic enter at stake, and similarly to the previous sections, reveals that the gate oxide layer has to be thick enough to guarantee an improvement of the interface quality, but not too much in order to avoid an outnumber of e-h pairs generated by irradiation that can highly alter the electrical properties (in term of stability) and shift the threshold voltage toward the negative values, as it is shown by the transconductance characteristics [Fig 3.36.a]. Still, the gate-source leakage current is not impacted by the irradiation [Fig. 3.36.b]. The μ_{fe} variation is 6 times higher after $5 \cdot 10^{13}$ cm^{-2} than in the NI samples (Table 3.11). However above this fluence, μ_{fe} value starts to decrease [Fig.3.36.c] due to lattice damage created during the irradiation process. As it can be seen, the fluence value that induces μ_{fe} decrease is two orders of magnitude higher than that of irradiated MOSFETs at 0.18 MeV (see Fig. 3.31.c) due to the deeper damage causing less negative effect at SiO_2/SiC interface.

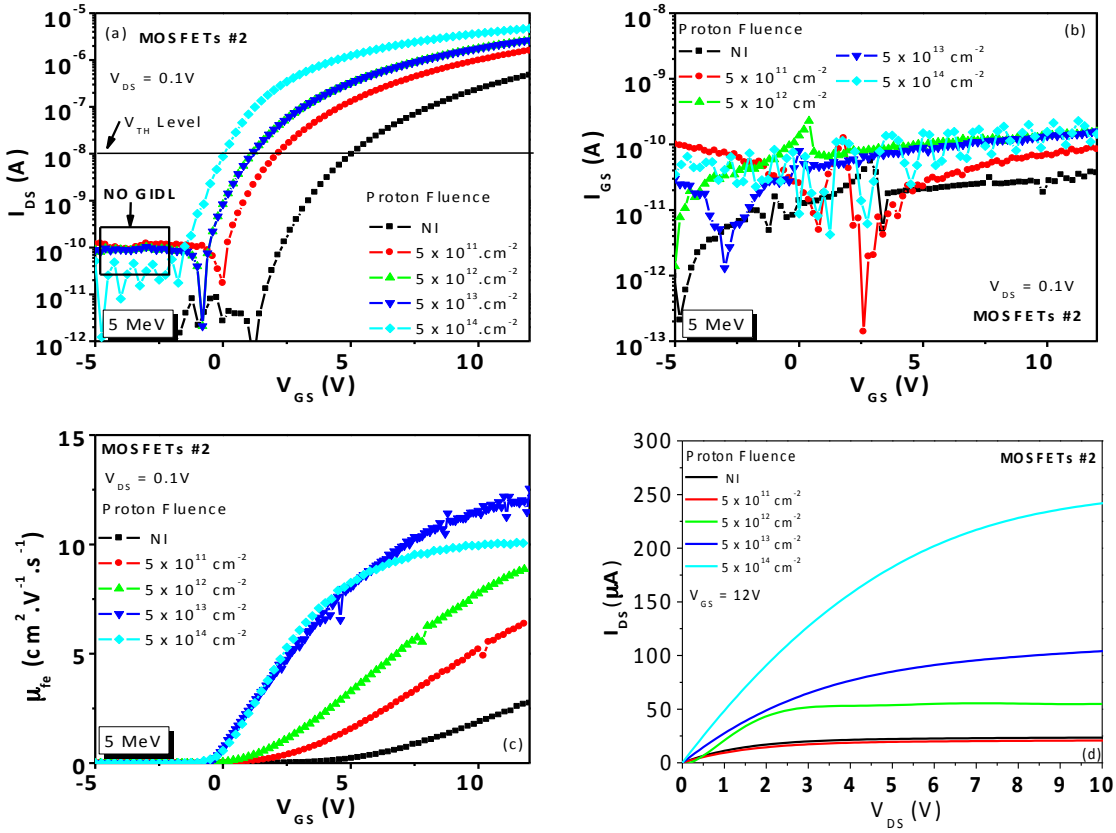


Fig 3.36 **Electrical characteristics of 5 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b), μ_{fe} (V_{GS}) (c) and I_{DS} (V_{DS}) at V_{GS} = 12V.**

BSI stress

The BSI analysis has shown very stable behaviour of the V_{TH_NBSI} values for all the irradiated samples [Fig 3.37.a]. ΔV_{TH} is almost equal to that of the NI MOSFETs after irradiation at all fluences, but its stability is much better, meaning that after 2 hours of time BS, ΔV_{TH} of the irradiated MOSFETs almost didn't change, remaining much closer to 0 that the ΔV_{TH} of the NI MOSFETs.

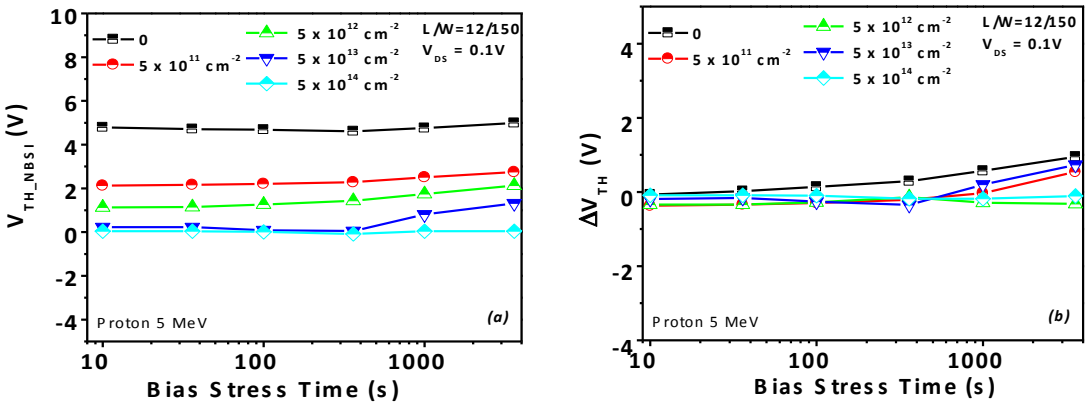


Fig 3.37. **Electrical characteristics of 5 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) V_{TH_NBSI} = f (t) at V_{ds} = 0.1 V (a) and ΔV_{TH} = f(t) (b).**

Other Parameters

As shown in Table 3.11, the absence of V_{oxide_br} increase with the fluence indicates that the additional oxide sublayer that could be created by the irradiation is negligible. The GIDL

Electrical Parameters	Non Irradiated	Proton Energy: 5 MeV			
		$5{\cdot}10^{11}$ cm^{-2}	$5{\cdot}10^{12}$ cm^{-2}	$5{\cdot}10^{13}$ cm^{-2}	$5{\cdot}10^{14}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ [V]	5.06	2.13	1.13	0.23	0.04
V_{oxide_br} [V]	47.2	46.3	47.2	43.6	47.5
$\mu_{fe\_Vg=12V}$ [cm^{-2}.V^{-1}s^{-1}]	2.70	2.11	9.08	13.78	10.3
$I_{D\_SAT\_MAX}$ [µA]	23.23	20.71	50.71	103.23	242.23
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert$[cm^{-2}]	0.040	0.209	0.192	0.107	0.051

Table 3.11. 4H-SiC n-MOSFET main electrical parameters before and after a 5 MeV proton irradiation at four different fluences.

variation with time is not impacted by the irradiation, its value and time behaviour being similar to that shown in Fig.3.17.c. Depending on the application type, the optimum irradiation process

than can be used for improving the EP of MOSFETs having an N_2O+TEOS gate oxide differs. For applications at room temperature, the MOSFET irradiation at $5\cdot10^{13}$ cm^{-2} could be a suitable solution for increasing its current capability while ensuring a normally-off behaviour. However, for higher temperatures, the negative threshold voltage shift is larger, and a fluence of $5\cdot10^{12}$ cm^{-2} is preferable for the sake of normally-off behaviour.

Time annealing impact

After extracting V_{TH_NBSI} on the PIA MOSFETs for the four irradiation fluences, we have observed a very clear recovery tendency (between 1V and 2V) of all the irradiated MOSFETs as it can be seen in Fig 3.38. a, b, c and d. The remarkable point is that the V_{TH_NBSI} instability is better in the PIA MOSFETs than that of the NI MOSFETs. However, in the case of PIA MOSFETs irradiated at $F=5\cdot10^{11}$ cm^{-2} and $F=5\cdot10^{12}$ cm^{-2}, the PIA process induced important ΔV_{TH} variation with time. Its ΔV_{TH} variation starts to be worse than that of the NI MOSFETs after applying a positive bias stress of 360s, as shown in Fig 3.39 .a and b. On the other hand, with higher irradiation fluences ($F=5\cdot10^{13}$ cm^{-2} and $F=5\cdot10^{14}$ cm^{-2}) the PIA MOSFETs ΔV_{TH} variation is much smaller than the previous one: they are almost equal to each other [Fig 3.39. c and d]. Except in the case of the PIA MOSFETs irradiated at $F=5\cdot10^{14}$ cm^{-2}, the μ_{fe} of the other PIA MOSFETs tend to recover with the annealing, although its values are much higher than the NI devices, as shown in Fig 3.40. a, b and c. It is suspected the e-h recombination to be predominant at fluences up to $5\cdot10^{13}cm^{-2}$. At $F = 5\cdot10^{14}cm^{-2}$, e-h recombination also occurred due to the V_{TH} recovery, but the slight N-diffusion may predominates as much as the e-h recombination due to the small μ_{fe} increase at V_{GS} = 12V with annealing time as observed in Fig 3.40.d. In addition, the μ_{fe} values are also much higher than the NI devices. It is worth to add that the nMOSFETs didn't show any type of leakage current after the PIA process. Table 3.12 summarizes the extracted values of the MOSFET's electrical parameters. The introduced charges $|N_{ox} + N_{it}|$ after the first cycle of BSI (T=10s) has shown reduced values in PIA MOSFETs irradiated at fluences up to $5\cdot10^{13}$ cm^{-2}, and, in the case of $F = 5\cdot10^{14}$ cm^{-2}, has shown negligible variations. However, for the PIA MOSFET irradiated at $F=5\cdot10^{12}$ cm^{-2}, the important ΔV_{TH} instability introduced a very high amount of positive effective

5 MeV Proton Fluence (p/cm^2)	**NI**	**$5\cdot10^{11}$**		**$5\cdot10^{12}$**		**$5\cdot10^{13}$**		**$5\cdot10^{14}$**	
		IRR	**ANN**	**IRR**	**ANN**	**IRR**	**ANN**	**IRR**	**ANN**
$V_{TH\_NBSI\_t=10s}$ (V)	5.06	2.13	3.83	1.13	3.01	0.23	1.34	0.04	1.76
V_{oxide_br} (V)	47.1	46.3	45.7	47.2	47.4	43.6	43.6	47.5	47.3
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	2.74	6.48	5.60	9.08	8.11	13.78	10.60	10.30	10.68
$I_{D\_SAT\_MAX}$ (µA)	23.24	20.71	29.5	4.03	24.9	103.24	75.8	242.23	167.9
$\|N_{ox} + N_{it}\|$ x 10^{12} cm^{-2}	0.040	0.209	0.074	0.192	0.079	0.107	0.034	0.051	0.060

Table 3.12. The extracted electrical parameters on irradiated at 5 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#2. NI= MOSFETs measured prior to irradiation.

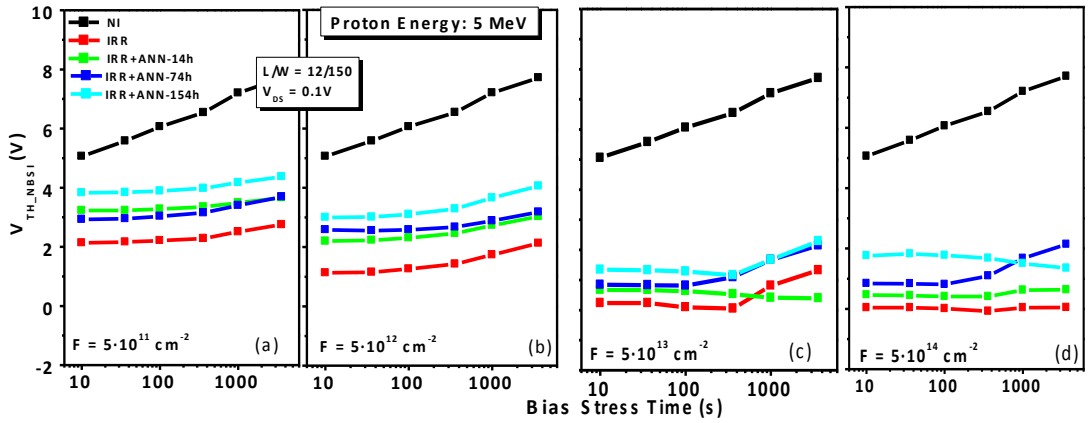


Fig 3.38. The threshold voltage time evolution after a NBS for 5 MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b), $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

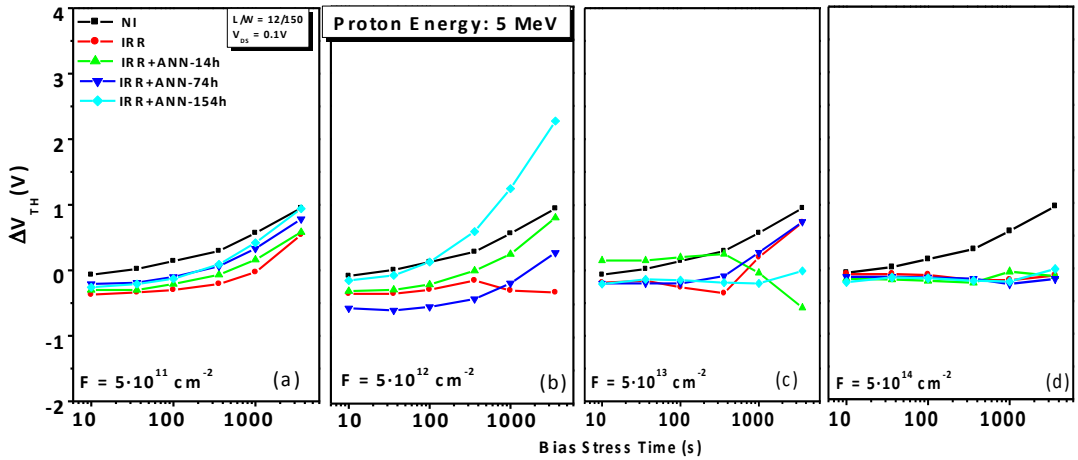


Fig 3.39. ΔV_{TH} time evolution for 5 MeV proton irradiated MOSFETS#2 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

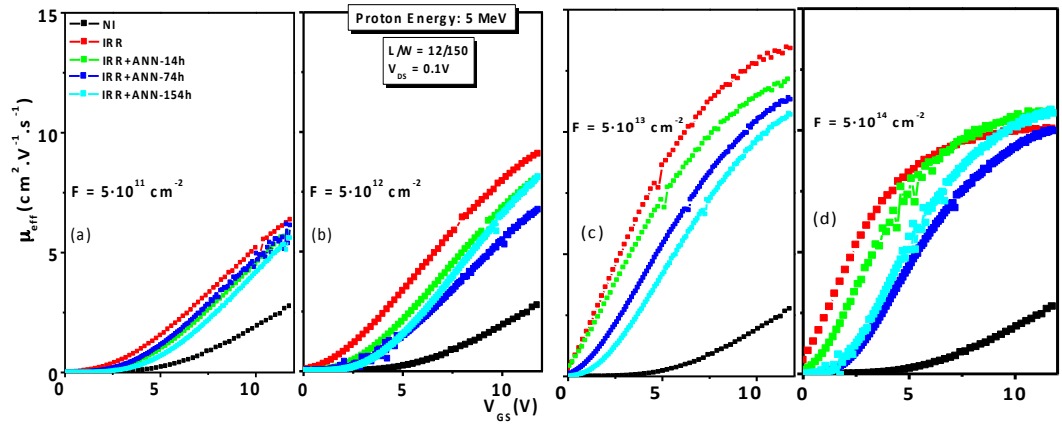


Fig 3.40. The field effect mobility time evolution after a NBS for 5 MeV proton irradiated MOSFETS#2 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

charge. This amount is about $1.27 \cdot 10^{12}$ cm^{-2} in this case whereas it do not overcome $5.3 \cdot 10^{11}$ cm^{-2} in all the other cases. The long term PIA annealing process didn't have any impact on the $V_{Oxide\_br.}$

3.5.3. High-Energy proton Irradiated MOSFETs

Effect of radiation fluence on the transconductance

Contrary to MOSFETs#1, the experimental results have shown that irradiated MOSFETs#2 under high proton energy only shift its transconductance characteristics toward negative values [Fig 3.41.a], accounting for a predominance of donors generated by irradiation at the SiO_2/SiC interface. MOSFETs#2 irradiated with the lowest fluence ($5 \cdot 10^{11}$ cm^{-2}) present a large gate leakage current (one order of magnitude higher than that of the other MOSFETs) that falsifies the extracted μ_{fe} value. Neglecting this fluence, the obtained μ_{fe} trend [Fig 3.41.c] presents a similar behaviour to the one observed in section 3.4.3 The irradiated MOSFETs at the highest fluence presented a μ_{fe} that is more than five times the value of the NI MOSFETs, and starts to saturate at V_{GS} = 10V. In the same manner, the irradiation fluence increase also raises $I_{D\_SAT\_MAX}$ [Fig 3.41.d].

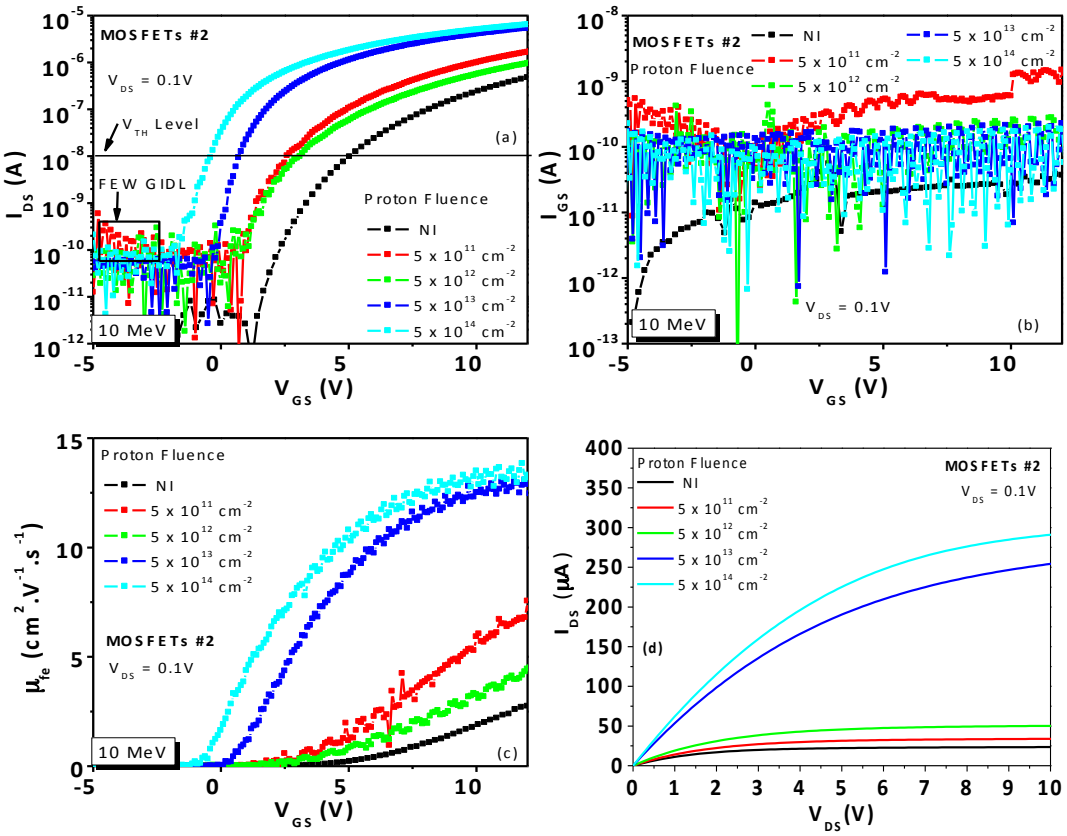


Fig 3.41 **Electrical characteristics of 10 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b), μ_{fe} (V_{GS}) (c) and I_{DS} (V_{DS}) at V_{GS} = 12V.**

BSI Stress

In addition, the V_{TH_NBSI} time shift of the transconductance characteristics is superior to that of the MOSFET#1 and may be related with the high irradiation energy (see section 3.3.3). The $I_{GS}(V_{GS})$ curves seemed to show a higher gate leakage current at a fluence of $5{\cdot}10^{11}$ cm^{-2} when compared to both the other irradiated MOSFETs at higher fluences and the NI MOSFET

[Fig 3.41.b]. This phenomenon also occurred in the case of irradiated MOSFETs#1 for the same proton fluence. The V_{TH_NBSI} stability of all irradiated MOSFETs is better than that of the NI MOSFET as shown in [Fig 3.42.a] and, similarly to the previous section, no significant GIDL current (>1 nA) has been detected during the BSI stress of all the irradiated MOSFETs. [Fig 3.42.b] shows the time ΔV_{TH} evolution accounting for introduced charges by BSI at the SiO_2/SiC interface. Contrary to section 3.4.3, the ΔV_{TH} instability is only worse for irradiated MOSFETs with $F=5{\cdot}10^{11}cm^{-2}$ compared to NI counterparts. Above this fluence, ΔV_{TH} time stability is better and the optimum value results for a fluence of $5{\cdot}10^{14}cm^{-2}$.

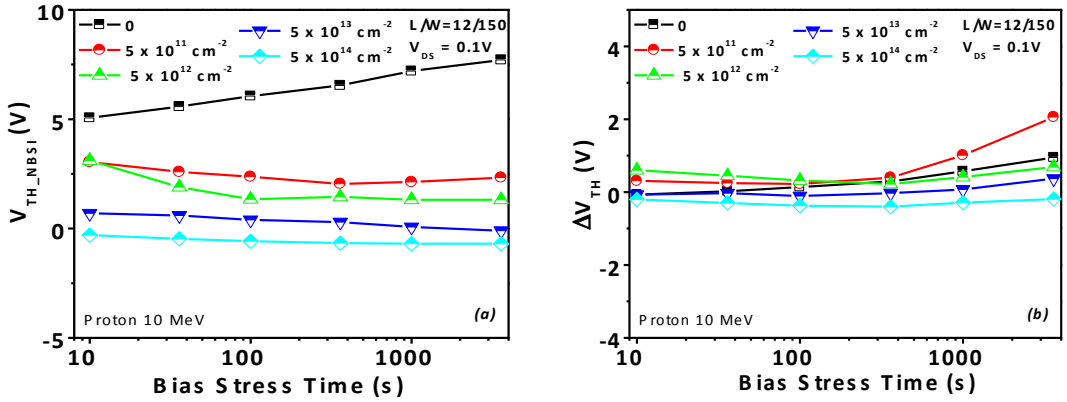


Fig 3.42. **Electrical characteristics of 10 MeV proton-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) $V_{TH\_NBSI} = f(t)$ at $V_{ds} = 0.1$ V (a), $\Delta V_{TH} = f(t)$ (b) and $\mu_{fe}(V_{GS})$ (c).**

Other Parameters

In table 3.13, the variation of the main electrical parameter is summarized. The optimum fluence that demonstrated the best EP improvement is $5{\cdot}10^{13}$ cm^{-2}. At a fluence of $5{\cdot}10^{14}$ cm^{-2}, even if ΔV_{TH} stability and μ_{fe} are improved, V_{TH} starts to be negative (normally-on behaviour) which must be avoided for a proper MOSFET operation.

Electrical Parameters	Non Irradiated	Proton Energy: 10 MeV			
		$5\cdot10^{11}$ cm^{-2}	$5\cdot10^{12}$ cm^{-2}	$5\cdot10^{13}$ cm^{-2}	$5\cdot10^{14}$ cm^{-2}
$V_{TH\_NBSI\_t=10s}$ [V]	5.06	3.04	3.11	0.61	-0.32
V_{oxide_br} [V]	47.2	47.2	46.2	48.2	45.5
$\mu_{fe\_Vg=12V}$ [cm^{-2}.V^{-1}s^{-1}]	2.70	6.80	5.56	13.4	13.6
$I_{D\_SAT\_MAX}$ [µA]	23.23	32.23	49.75	254.33	292.77
$\lvert N_{it} + N_{ox} \times 10^{12}\rvert$[cm^{-2}]	0.040	0.175	0.340	0.0396	0.113

Table 3.13 4H-SiC n-MOSFET main electrical parameters before and after a 10 MeV proton irradiation at four different fluences.

Time annealing impact

In this case, long time PIA annealing process induced a very small V_{TH_NBSI} recovery, and improved the time stability of all PIA MOSFETs [Fig 3.43.a,b,c and d]. At long time BS, V_{TH_NBSI} values start to show small variations. However these variations, although higher than that of the irradiated MOSFETs, are lower than that of the NI samples. Nevertheless, what is critical in this situation is the ΔV_{TH} variation. Indeed, for the case of PIA MOSFET irradiated at F = $5\cdot10^{11}$ cm^{-2}, and despite the ΔV_{TH} stability increase in comparison with the irradiated MOSFETs, the annealing process still induced a decrease of the ΔV_{TH} time stability in comparison with the NI MOSFET [Fig 3.44.a]. In this situation, it means that additional holes couldn't fully recombine with the electron during the PIA process: Most of them may have been trapped during the irradiation, and the annealing process wasn't enough to induce hole detrapping with a subsequent recombination with electron. In the case of PIA MOSFETs irradiated with F = $5\cdot10^{12}$ cm^{-2} and $5\cdot10^{13}$ cm^{-2}, the ΔV_{TH} have shown very unstable values: Its stability which has been improved after the irradiation process has become worse than that of the NI MOSFETs [Fig 3.44.b and c]. For F = $5\cdot10^{12}$ cm^{-2}, the $|N_{ox} + N_{it}|$ value reaches a value of $1.28\cdot10^{12}$ cm^{-2} after a time BSI of 3600s, which correspond to the double of the NI MOSFETs value at the same time BS period. This instability did not occur in the case of MOSFET#1, meaning that the main reason of the ΔV_{TH} variation might be connected to the thicker oxide. Indeed, with a thicker oxide, the amount of e-h pair generated within the oxide is higher. Thus, during either irradiation or annealing process, the amount of generated charges that might be trapped at the SiO_2/SiC interface is higher in MOSFETs#2. Thus, the probability of having V_{TH} instability is higher in MOSFET#2. However, for F = $5\cdot10^{14}$ cm^{-2}, the ΔV_{TH} stability is much better than that of both the irradiated and NI MOSFETs [Fig 3.44.d]. The reason of the stability at F = $5\cdot10^{14}$ cm^{-2} is not fully understood. Perhaps, due to the small μ_{fe} increase at this fluence [Fig 3.45.d], it can be suggested that the N-diffusion was the predominant phenomenon. If we take a look at what happen at lower fluences, the μ_{fe} values tend to recover in all the cases [Fig 3.45. a, b and c],

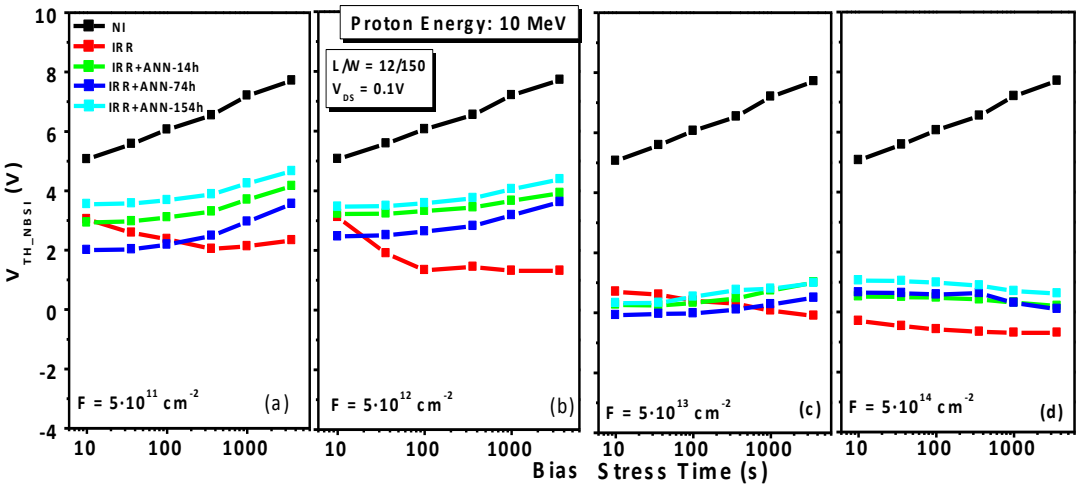


Fig 3.43. The threshold voltage time evolution after a NBS for 10MeV proton irradiated MOSFETS#1 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}\,cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

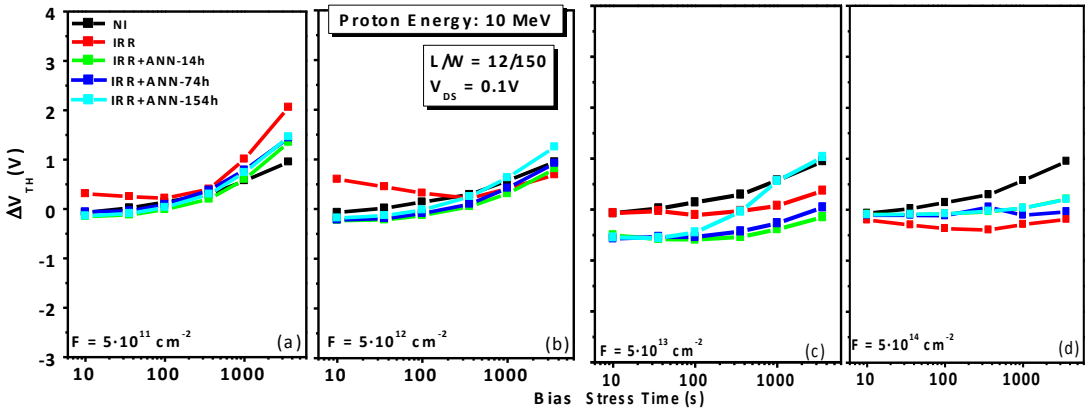


Fig 3.44. ΔV_{TH} time evolution for 10 MeV proton irradiated MOSFETS#2 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}cm^{-2}$ (b) and $5{\cdot}10^{13}cm^{-2}$ (c) and $5{\cdot}10^{14}\,cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

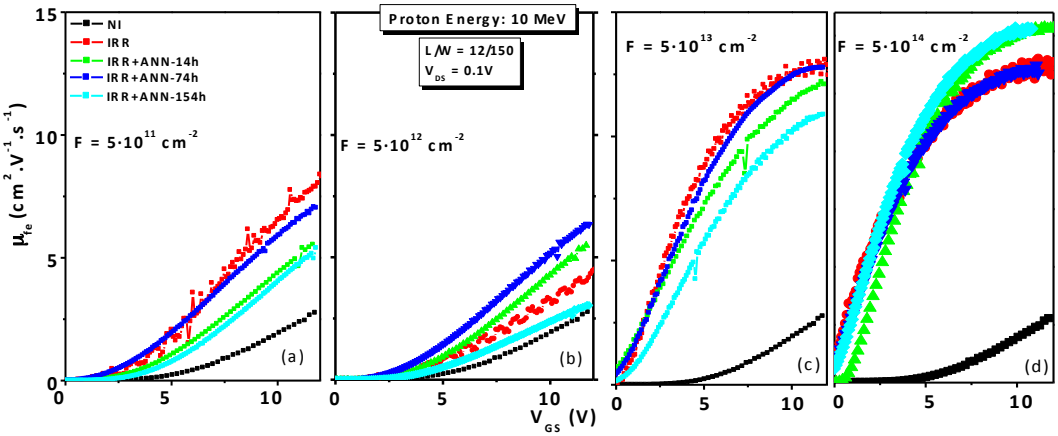


Fig 3.45. The field effect mobility time evolution after a NBS for 10 MeV proton irradiated MOSFETS#2 at $5{\cdot}10^{11}cm^{-2}$ (a), $5{\cdot}10^{12}\,cm^{-2}$ (b), $5{\cdot}10^{13}\,cm^{-2}$ (c) and $5{\cdot}10^{14}\,cm^{-2}$ (d) after irradiation and several time annealing (14h, 74h and 154h).

10 MeV Proton Fluence (p/cm^2)	NI	$5\cdot10^{11}$		$5\cdot10^{12}$		$5\cdot10^{13}$		$5\cdot10^{14}$	
		IRR	ANN	IRR	ANN	IRR	ANN	IRR	ANN
$V_{TH\_NBSI\_t=10s}$ (V)	5.06	3.04	3.55	3.11	3.46	0.70	0.32	-0.30	1.05
V_{oxide_br} (V)	47.1	47.2	47.1	46.2	46.1	48.2	47.5	45.5	45.2
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	2.74	6.80	5.39	8.01	3.03	12.93	10.87	13.6	14.89
$I_{D\_SAT\_MAX}$ (µA)	23.24	32.23	29.2	49.75	35.9	225.33	186.6	292.77	237.4
$\lvert N_{ox} + N_{it}\rvert$ x 10^{12} cm^{-2}	0.04	0.175	0.049	0.34	0.050	0.039	0.152	0.113	0.03

Table 3.14. The extracted electrical parameters on irradiated at 10 MeV proton energy for different fluences, and PIA 4H-SiC MOSFETs#2.

meaning that the e-h recombination might the predominant process during the annealing. V_{OXIDE_BRR} didn't show any variation after the annealing process [Table 3.14], and $I_{D\_SAT\_MAX}$ at V_{GS}=12V of PIA MOSFETs shown values as expected.

3.5.4. Bias Temperature Instability Impact

The different types of phenomena observed in section 3.4.4 are also founded in the frame of the temperature annealing study of PIA of MOSFET#2. The first one is the very peculiar threshold voltage hump observed with the temperature increase is not only observed on several PIA MOSFETs#1 (as it was the case in section 3.4.4, but also on the majority of the PIA MOSFETs#2. They are plotted on Fig 3.46.a, b, and c. Thus, in most of the cases, V_{TH} starts to decrease with the temperature increase in the range of [25ºC; 100ºC], then it increases within the temperature range of [100 ºC ; 175ºC]. Above 175ºC, the V_{TH} decrease is observed. As already discussed in the section 3.4.6, the abrupt V_{TH} variation with temperature might be connected to deep level traps that are activated within the temperature range of [100 ºC; 175ºC].

The second effect has been observed on the NI MOSFETs that has shown a μ_{fe} peak overcoming 500 $cm^{-2}.V^{-1}.s^{-1}$ when V_{GS} = 2V [Fig 3.47.a]. This peak has been also observed in the frame of the study of electron impact on 4h-SiC MOSFET (see chapter 4). At this gate voltage, the leakage current is lower than 1 nA. Moreover, this high μ_{fe} value is a real one since more than 3 experimental points are above 450 $cm^{-2}.V^{-1}.s^{-1}$ and more than 10 are above 300 $cm^{-2}.V^{-1}.s^{-1}$. However, at V_{GS} >12V, μ_{fe} values collapse due to the roughness scattering predominance on the other effects, being around 18 $cm^{-2}.V^{-1}.s^{-1}$. Now let's go back to the study of PIA MOSFETs#2. The roughness correction induced by irradiation is also shown in this case [Fig 3.47.d], where a clear saturation of μ_{fe} is observed at 200ºC for PIA MOSFETs irradiated at 0.18 MeV with F = $5\cdot10^{13}$ cm^{-2}. Moreover, at 250ºC and at V_{GS} > 12V, μ_{fe} tends to be around 25 $cm^{-2}.V^{-1}.s^{-1}$, which is 67% better that that of the NI MOSFETs. We suggest this phenomenon to be related with a lower roughness scattering. The measured μ_{fe} values at high gate voltages are remarkable higher than those obtained for MOSFETs#1 due to the thicker gate oxide. This behaviour has also been founded at other fluences. In all the experiments, μ_{fe} values at high temperature and at V_{GS} > 12V tend to the same values, being in that case around 35 $cm^{-2}.V^{-1}.s^{-1}$. A similar tendency is observed in the case of PIA MOSFETs irradiated at 5 MeV and 10 MeV (Fig 3.47.b and c).

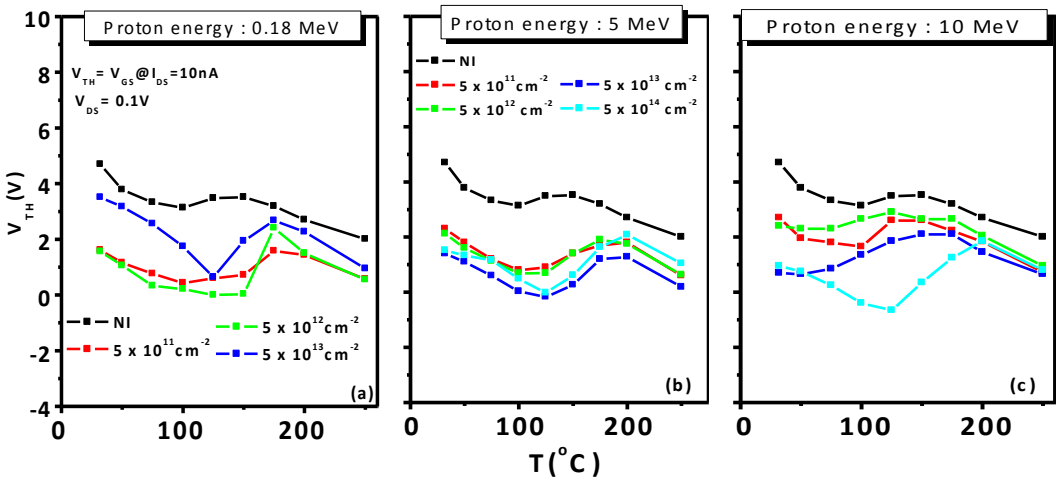


Fig 3.46. The V_{TH} temperature evolution for the NI MOSFETs and PIA MOSFETs of all fluences and fluences at a proton irradiation of 0.18 MeV (a), 5 MeV (b) and 10 MeV (c), respectively.

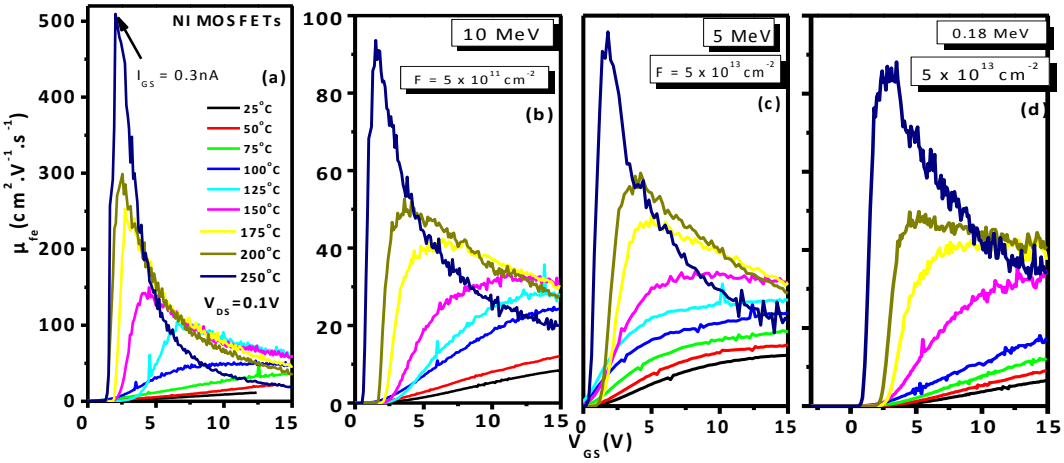


Fig 3.47. Evolution of the effective channel mobility with the increase of temperature for non-irradiated (a) and PIA MOSFETs irradiated at 10 MeV with a proton fluence of $5{\cdot}10^{11}$ cm^{-2} (b), at 5 MeV with a proton fluence of $5{\cdot}10^{12}$ cm^{-2} (c), at 0.18 MeV with a proton fluence of $5{\cdot}10^{13}$ cm^{-2} (d).

3.5.5. Conclusion on irradiated MOSFETs having a N_2O + TEOS gate oxide

Irradiation of MOSFETs having a N_2O+TEOS gate oxide has allowed to point out different problematics related to the charge build-up mechanism. Especially, the V_{TH} behaviour has shown that there is a trade-off to find between the gate oxide thickness, the thickness of the $N_xS_yO_z$ /$N_xC_yO_z$ transition layer and the irradiation fluence and energy if we want to improve the MOSFETs EP by irradiation. In general, no significant gate leakage current and no GIDL have been observed on the irradiated MOSFETs. Thus, their oxide breakdown voltage values didn't really change (except in the case of low proton irradiated MOSFETs at $5{\cdot}10^{13}$ cm^{-2}). Low proton irradiation energy at high fluence, as well as high energy electron irradiation at high fluence can really degrade the oxide. Depending on the irradiation energy, a specific conclusion has been draft.

Post-irradiation annealing performed on MOSFET#2 having N_2O+TEOS gate oxide has shown very serious threshold voltage hysteresis instability issues. These issues are not very well understood, and they seem occurring at random irradiated fluence. The experiment put in evidence that the probable cause of the V_{TH} instability observed is related either to the oxide thickness or to the amount of generated interface charges within the interface transition layer. It is suggested that, with a thick oxide, the amount of e-h generated by irradiation is superior to the ones generated in a thin oxide. Thus, instabilities due to charge issues can occur with much probability and might be enhanced by the annealing process. A positive impact of N_2O + TEOS gate oxide (MOSFETs#2) is that the interface roughness at high temperature annealing that, in some cases, has been improved, and, contrary to MOSFET#1, has shown a much better μ_{fe} at high V_{GS}. In any cases, there is no detection of any sort of leakage. Moreover, the oxide breakdown voltage remained equal for all the irradiated and non-irradiated devices. A specific summary can be draft for each case.

Low proton irradiation energy: This experiment confirms the existence of a threshold fluence (F_{TH}) from which a change of the predominating charges from donor to acceptor at the SiO_2/SiC interface occurs. It also show that, at low irradiation energies, the thicker the gate oxide the higher the amount of generated e-h pairs in the oxide and the more predominant the acceptor traps during the BSI measurement. The best results that combine an improvement of the MOSFETs V_{TH} stability together with the increase of μ_{fe} and $I_{D\_SAT\_MAX}$ have been obtained for an irradiation fluence of $5 \cdot 10^{11}$ cm^{-2}. However, MOSFETs#1 having a N_2O gate has shown a better time stability of the $V_{TH,}$ probably due to the thicker $N_xS_yO_z$ /$N_xC_yO_z$ transition layer that may compensate the irradiation damages in the epilayer.

PIA Process : At long time of PIA, the ΔV_{TH} instability is only detected at F = $5 \cdot 10^{12}$ cm^{-2} and not at higher fluence. For this fluence, the μ_{fe} has even been improved together with the decrease of V_{TH}. This may be due to an additional N-diffusion together with holes moving within the oxide. At F = $5 \cdot 10^{11}$ cm^{-2} and F = $5 \cdot 10^{13}$ cm^{-2}, the e-h recombination together with the charge trapping/detrapping are the predominant effects due to the V_{TH} recovery. The V_{TH} variation follows the same trend as the one observed in the NI case. Moreover at all irradiated fluences, an increase of surface roughness quality have been observed due to the μ_{fe} behaviour values.

Medium proton irradiation energy: The experimental results allowed once again showing the oxide thickness impact on the MOSFETs threshold voltage drift. Indeed, due to its very thick gate oxide, the V_{TH} values drastically decreased after irradiation and kept on decreasing with the increase of the fluence. What is specific to this irradiation energy concern the V_{TH} time stability, which has been improved in comparison with the NI MOSFETs. A similar V_{TH} and ΔV_{TH} stability of the irradiated MOSFETs#2 to that of MOSFETs#1 has been observed, and the μ_{fe} and $I_{D\_SAT\_MAX}$ capability increased with the increase of the fluence. The best results in term of trade-off between the decrease of V_{TH} values, the V_{TH} stability, μ_{fe} and $I_{D\_SAT\_MAX}$ is obtained for a proton fluence of $5 \cdot 10^{12}$ cm^{-2}.

PIA Process : Despite of the ΔV_{TH} instability occurring for an unclear reason at F = $5 \cdot 10^{12}$ cm^{-2}, a clear recovery tendency of the V_{TH_NBSI} has been observed, and the ΔV_{TH} time stability obtained after irradiation has been kept at F=$5 \cdot 10^{13}$ cm^{-2} and F = $5 \cdot 10^{14}$ cm^{-2}. This account for the predominance of e-h recombination. The μ_{fe}, for irradiated fluences up to $5 \cdot 10^{13}$ cm^{-2} has shown recovery tendency whereas it slightly increased at $5 \cdot 10^{14}$ cm^{-2}, accounting for a small N-diffusion together with the e-h recombination. The high temperature annealing process has shown at V_{GS} > 12V and T = 250ºC similar values than that of the NI MOSFETs.

High proton irradiation energies : The behaviour of the MOSFETs#2 EP revealed that either high energy proton (or high energy electron) irradiation beam induces a smaller V_{TH} decrease when increasing the fluence compared to MOSFETs#1. MOSFETs#2 irradiated under high proton energies have shown better ΔV_{TH} stability for all irradiated fluences than that of MOSFETs#1. The optimum irradiation fluence that contributed to improve most of MOSFETs main EP is between $5 \cdot 10^{12} cm^{-2}$ and $5 \cdot 10^{13} cm^{-2}$. Above $5 \cdot 10^{13} cm^{-2}$, V_{TH} starts to be negative.

PIA Process: The e-h recombination also occurred and recover the V_{TH_NBSI} and μ_{fe} values to the NI ones for fluences up to $5 \cdot 10^{13}$ cm^{-2}. However, instability issues of ΔV_{TH} occurred for the PIA MOSFETs irradiated with a fluence up to $5 \cdot 10^{13}$ cm^{-2} and are connected to the e-h recombination and charge trapping/detrapping effect that cannot be separated from the e-h recombination. The thermal behaviour obtained in the frame of the BTI stress is the same as the one obtained after irradiation at 5 MeV. The only difference is the V_{TH} increases at F = $5 \cdot 10^{14}$ cm^{-2} in the temperature range of [125ºC; 200ºC], which is higher in the case of PIA MOSFETs#2 irradiated at 10 MeV. It is suspected in this case that 10 MeV proton beam provoke more damage of the epilayer crystal lattice than that of the 5 MeV, inducing deep level traps that activates at high temperature.

3.6 General conclusion

4H-SiC MOSFETs with an oxynitrided gate oxide have shown an proton irradiation robustness behaviour. It has been shown that irradiation process could even be considered as an additional process for MOSFET fabrication because it optimizes in some cases the MOSFETs main electrical parameter. It can also be used as a reliability test in order to determine the MOSFETs gate oxide robustness. The poor quality of the processed MOSFET allowed showing several positive impact of proton irradiation on the MOSFETs main electrical parameters. Proton and beam can, with a suitable fluence and energy, improve the threshold voltage stability, increase the current capability and the field effect mobility of a 4H-SiC MOSFETs having an oxynitrided gate oxide. Nevertheless, some limitations that depend on the dielectric layer process regarding the electrical behaviour have been founded. These limitations may be due to the poor SiO_2/SiC interface quality of 4H-SiC MOSFETs prior to irradiation. Thus, one solution to improve the irradiated MOSFETs electrical performances may be to perform an

annealing process. Thus analysis of, the post irradiation annealed MOSFETs having different gate oxide, under different time and different temperature has been carried out and compared. The effect of the annealing process has been identified. Several issues generally connected to the time ΔV_{TH} variation and the time and temperature V_{TH_NBSI} variation with time and temperature has been discussed. Nevertheless, the deep understanding of the phenomenon previously described is still under investigation and remains as an open issue.

3.7 References

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Chapter 4

Electron Irradiation of 4H-SiC MOSFETs with Oxynitrided Gate Oxide

In this chapter, the impact of electron irradiation on 4H-SiC MOSFETs is presented. Electrical parameters of irradiated MOSFETs having similar gate oxide as the ones presented in the previous chapter are shown. Time and temperature instability of the threshold voltage due to the post irradiation annealing process have been founded to be worse than that of proton irradiation. In addition one single event with a proper behavior that does not follow the global trend is reported.

4.1. The electron irradiation experiment

Electron is a particle which is 1770 times lighter than a proton. It can be easily produced by collision of particles with the material and by thermal excitation of the lattice structure. Electrons are also present in the radiation environment and can interact in two different ways with the material they are colliding: Coulomb interaction and scattering with the nucleus, the latter as in the case of a proton irradiation. The today lack of information in the state-of-the-art about electron irradiation impact on 4H-SiC MOSFETs is the main reason of the study. In the space application, electron radiation play a primary role. The Earth is surrounded by two doughnut-shaped regions [1] of energetic electrons [Fig 4.1], trapped in the Earth's magnetic field, and known as the Van Allen electron radiation belts. The inner belt, which extends from 1,200 km to 6,500 km above the surface of the Earth, is relatively stable whereas the outer belt, which extends from 13,000 km to 40,000 km, is highly variable. The belts are usually separated by a gap, known as the slot region which contains very few energetic electrons. In the highly dynamic outer belt, the fluxes change dramatically and may vary by up to five orders of magnitude on timescales of several hours to a few days. Thus, electron irradiation harshness component is a primary importance.

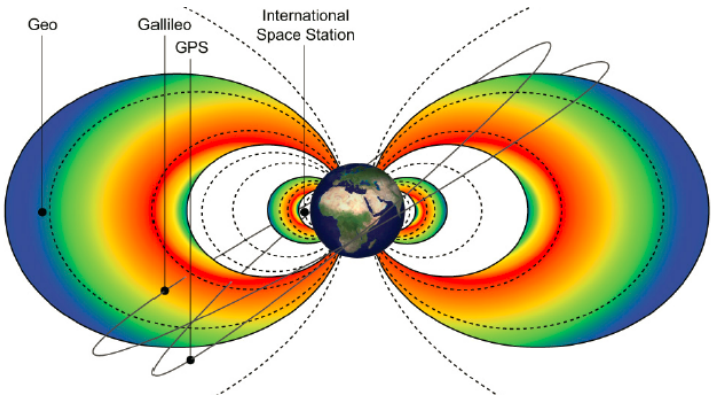

Fig 4.1. Representation of the inner and outer irradiation belt together with satellite orbital

The irradiation set up decided for the experiment is defined in table 4.1 and has been carried out at high energy on both MOSFET#1 and MOSFET#2 types.

Particle type	Electron
Energy (MeV)	15
kGy	Mrad
1	0.1
10	1
20	2
30	3

Table 4.1. Summary of the electron irradiation parameters used in the experiment: energy and dose performed on the two different batches of SiC-MOSFETs (N_2O RTP and N_2O RTP + TEOS gate oxide).

It is reminded that, as in chapter 3, the presented results have been obtained on 4 different MOSFETs of the different designs that, before irradiation, after irradiation in similar irradiation conditions, have shown repeatable behavior.

4.2. High-Energy Electron Irradiated MOSFET having a N_2O Gate oxide

4.2.1 Global analysis

Effect of radiation dose on the transconductance

MOSFET irradiation under electron beam at high energy (15 MeV) allows studying the impact that can be transfer to the oxide and crystal lattice integrity, just by crossing electrons through the MOSFETs at high speed. The first observation is that, as seen for proton irradiation, the electron irradiation induces a negative shift of the transconductance characteristics and, as a consequence, of the threshold voltage V_{TH}. Moreover, when compared to the NI MOSFETs, the electron irradiation caused an additional slight negative drift of the I_{DS} (V_{GS}) curves after each NBSI stress [Fig. 4.2.a], accounting for a predominance of donors traps at the SiO_2/SiC interface. However, this shift does not follow a clear trend. Indeed for the lowest absorbed dose (1 kGy), the transconductance shift is higher than the one of the irradiated samples at 10 kGy and 20 kGy. However, considering the different measurements performed on this study, we finally considered the case of 1 kGy as a single event and excluded it from the analysis. Regarding other parameters, it is noticeable that the electron irradiation didn't induce any gate leakage, as seen in [Fig.4.2.b]. This fact demonstrates the high robustness of the oxinitrided gate oxide. In comparison with the NI MOSFETs, μ_{fe} increases with electron irradiation [Fig. 4.2.c], and reaches four times the NI value at the highest absorbed dose (30 kGy).

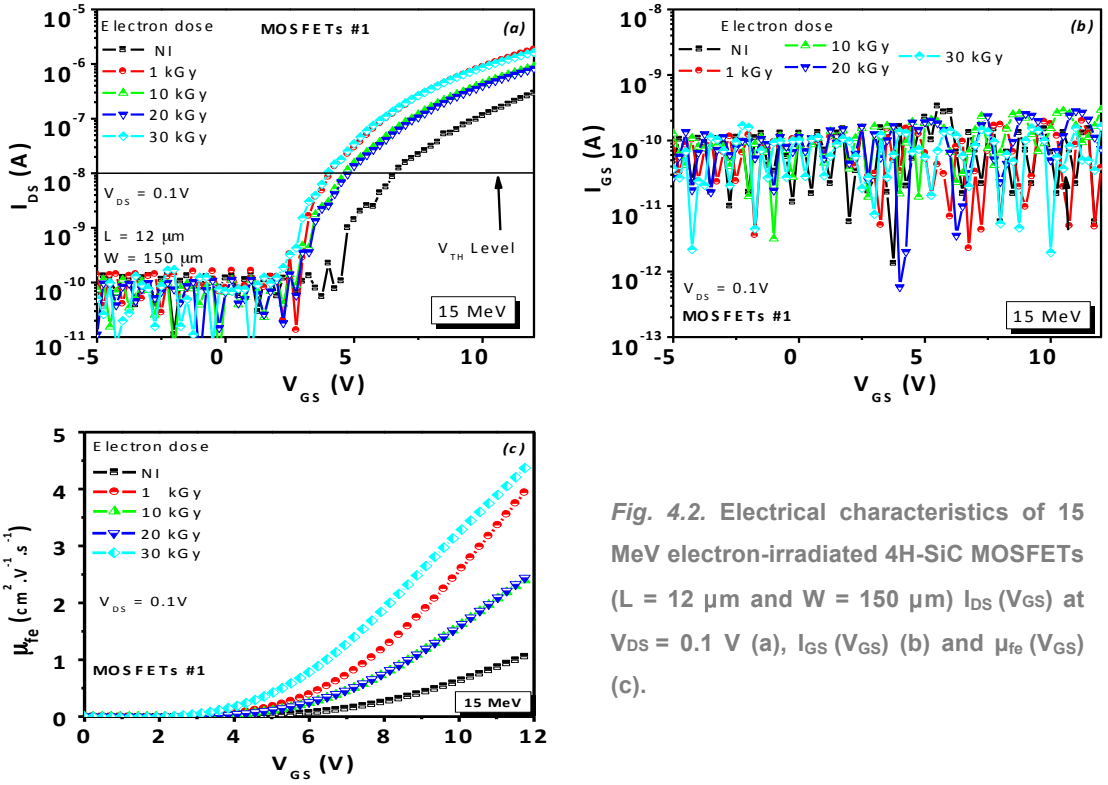

Fig. 4.2. **Electrical characteristics of 15 MeV electron-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b) and μ_{fe} (V_{GS}) (c).**

BSI stress

BSI tests have been performed on the electron irradiated SiC MOSFETs. The I_{DS} (V_{GS}) characteristics for 30 kGy absorbed dose have been extracted [Fig.4.3.b] and compared with that of the NI MOSFETs [Fig 4.3.a]. It can be seen that the observed behavior is similar to that previously observed for proton irradiation. At 30kGy, experimental results exhibit both a lower V_{TH_NBSI} [Fig.4.4.a] and V_{TH_PBSI} variation with stress time, resulting in a more stable ΔV_{TH} drift. ΔV_{TH} decreases gradually with the increase of the irradiated dose, and gets stabilized at the highest irradiation dose [Fig. 4.4.b]. Moreover, at this dose, the oxide charge trap and interface state charges generated by the BSI stress is 5 times lower than in the NI MOSFETs

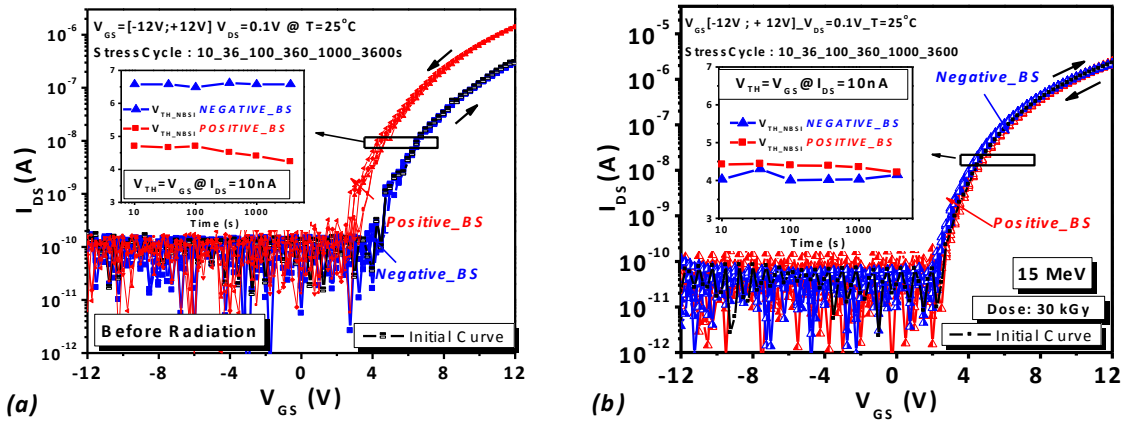

Fig. 4.3. n-MOSFET Threshold voltage evolution versus time during the BSI test. (a) For a non-irradiated sample and (b) for a 15 MeV $5 \cdot 10^{14}$ cm^{-2} electron irradiated MOSFET

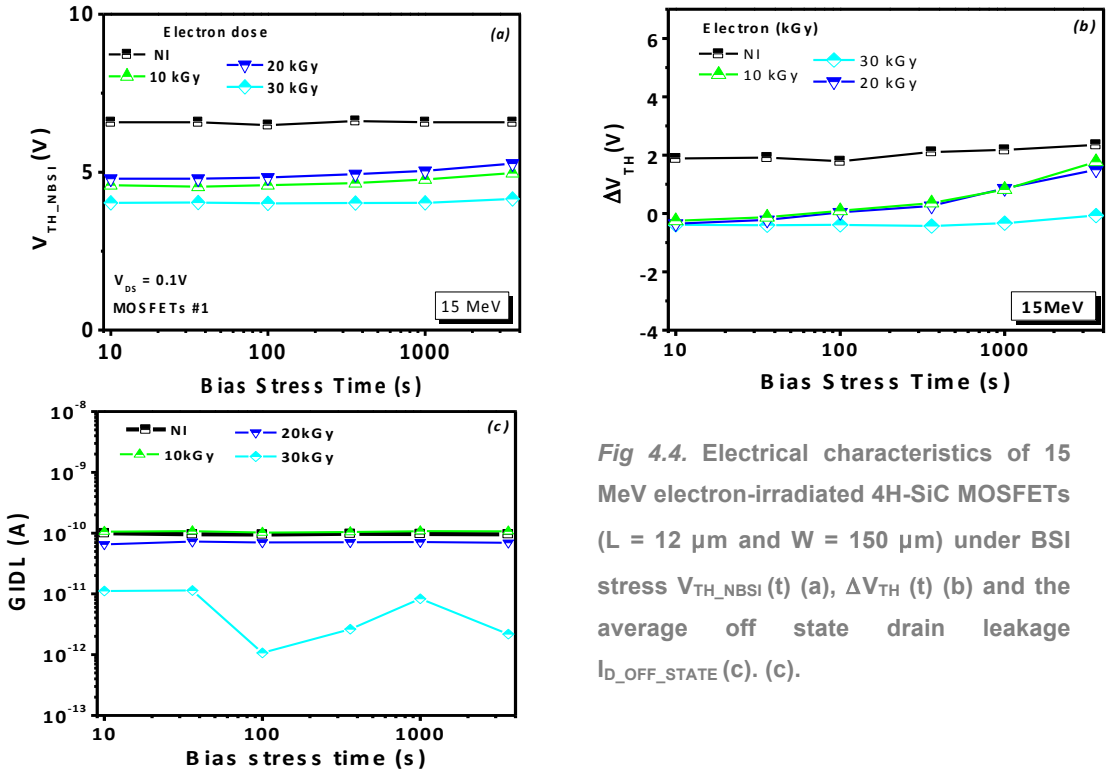

Fig 4.4. **Electrical characteristics of 15 MeV electron-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) under BSI stress V_{TH_NBSI} (t) (a), ΔV_{TH} (t) (b) and the average off state drain leakage $I_{D\_OFF\_STATE}$ (c). (c).**

(see Table 4.2). Finally, the I_{DS} (V_{GS}) curves exhibit similar GIDL [Fig 4.4.c] when compared with the NI MOSFETs.

Other Electrical Parameters

In addition, the $I_{D\_Max\_SAT}$ of the irradiated MOSFETs at 30kGy increased approximately two times in comparison with the NI MOSFETs. Then, irradiated MOSFETs at 30kGy seemed to show an improvement of all the electrical characteristics: time stability, effective channel mobility increase, noticeable rise of the $I_{D\_SAT\_MAX}$, and even an oxide breakdown voltage increase. These results do not completely fit with the classical irradiation theory established for Si-MOSFETs, since this theory is based on a dielectric layer only made by SiO_2, unlike our SiC MOSFETs made with oxinitrided gate dielectric.

Electrical Parameters	Non Irradiated	Electron Energy: 15 MeV		
		10 kGy (Si)	20 kGy (Si)	30 kGy (Si)
$V_{TH\_NBSI\_t=10s}$ [V]	6.58	4.59	4.79	3.83
V_{oxide_br} [V]	23.56	26.54	27.21	23.64
$\mu_{fe\_Vg=12V}$ [$cm^2.V^{-1}s^{-1}$]	1.20	2.59	2.42	4.32
$I_{D\_SAT\_MAX}$ [µA]	15.33	11.50	8.66	26.93
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert$ [cm^{-2}]	1.06	0.41	0.21	0.23

Table 4.2. 4H-SiC MOSFET main electrical parameters before and after 15 MeV electron radiations at four different electrons absorbed doses.

4.2.2. Bias Temperature Instability Impact

As in the previous chapter, we performed annealing under N_2 at 120ºC for 14, 84 and 154 h to study the recovery mechanism. The MOSFETs were measured after irradiation and after each annealing step, using the BSI technique and following the cycle defined in section 2.6. After the final annealing, they were measured under BTI, from 25ºC to 250ºC For all the electrons absorbed doses, the V_{TH_NBSI} exhibited almost no recovery after annealing, as presented in [Fig 4.5. a, b, c and d]. The very small recovery tendency observed in the case of the PIA MOSFETs irradiated at F= 10kGy and F= 30kGy does not allow to make any conclusion about the recombination predominance during the annealing. The lack of recovery observed (as also observed in several cases of the previous sections) may be due to an insufficient annealing temperature that does not allow the e-h recombination to occur. It was not possible to perform any annealing at temperatures higher than 120ºC because, as mentioned in the previous chapter, the MOSFETs were pasted on a Si wafer carrier using a carbon tape material which starts decomposing at 140ºC [2].

On the other hand, the very high instability observed in the case of irradiated MOSFETs at 1 kGy is enhanced with annealing time [Fig 4.6.a]. In this case, it is suggested that the positive bias stress induces either charge detrapping of electron within the oxide, or charge tunneling from the epilayer to the oxide followed by an in-situ trapping within the oxide. Thus, at low doses, the annealing degrades V_{TH} stability and increases ΔV_{TH}. At doses of 10 kGy and 20 kGy, this ΔV_{TH} degradation with time does not seem to occur, as shown in [Fig 4.6.b] and [Fig 4.6.c], respectively. On the contrary, it seems that the annealing time even improved the ΔV_{TH} stability, as in case of PIA MOSFETs proton irradiated at 10 MeV. The justification of such a behavior is given in section 3.4.6. Finally, For the PIA MOSFETs that have been irradiated with a dose of 30 kGy, the short time annealing firstly improved the ΔV_{TH} stability, before making it worse with the increase of the annealing time.

Thus, in the case of electron irradiation of MOSFETs having an N_2O oxynitrided gate oxide, it has been shown that the post irradiation annealing may exhibit “charge neutralized effect” for a specific irradiation dose (in our case 30 kGy), but the recovery effectiveness of this annealing may be limited by the charge trapping-detrapping effect during the time BSI stress. The MOSFETs μ_{fe} didn’t present significant variation after the longest PIA time: Their values

15 MeV Electron absorbed dose (kGy)	**NI**	**10**		**20**		**30**	
		IRR	**ANN**	**IRR**	**ANN**	**IRR**	**ANN**
$V_{TH\_NBSI\_t=10s}$ (V)	6.58	4.59	5.29	4.79	4.99	3.83	4.37
V_{oxide_br} (V)	23.42	26.54	26.40	27.21	27.10	23.64	23.30
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	1.20	2.59	1.75	2.42	2.44	4.32	3.98
$I_{D\_SAT\_MAX}$ (µA)	15.04	11.50	10.04	8.66	9.90	26.93	14.07
$\lvert N_{ox} + N_{it} \rvert$ x 10^{12} cm^{-2}	1.06	0.41	0.18	0.21	0.18	0.23	0.14

Table 4.3. The extracted electrical parameters on irradiated at 15 MeV electron energy for different doses, and PIA 4H-SiC MOSFETs#1.

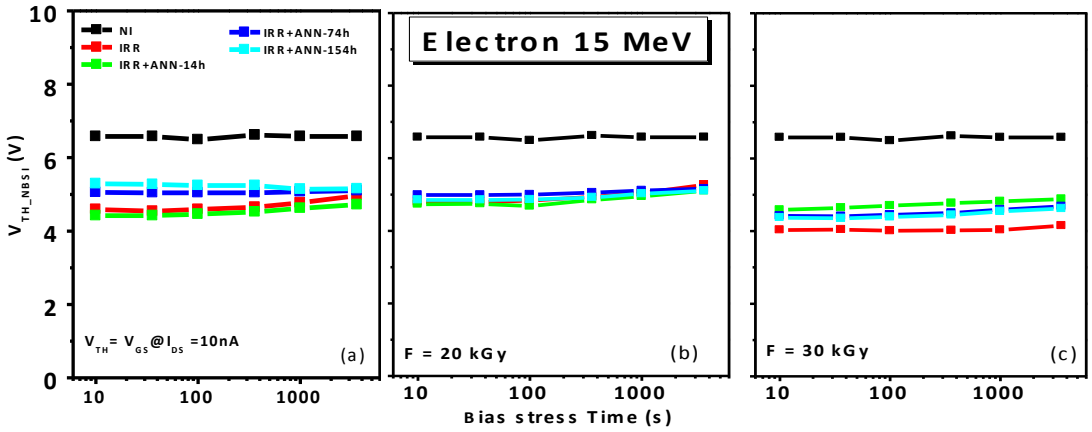

Fig 4.5. The threshold voltage time evolution after a NBS for 15 MeV electron irradiated MOSFETS#1 at 10kGy (a), 20 kGy (b) and 30 kGy (c) after irradiation and several time annealing (14h, 74h and 154h).

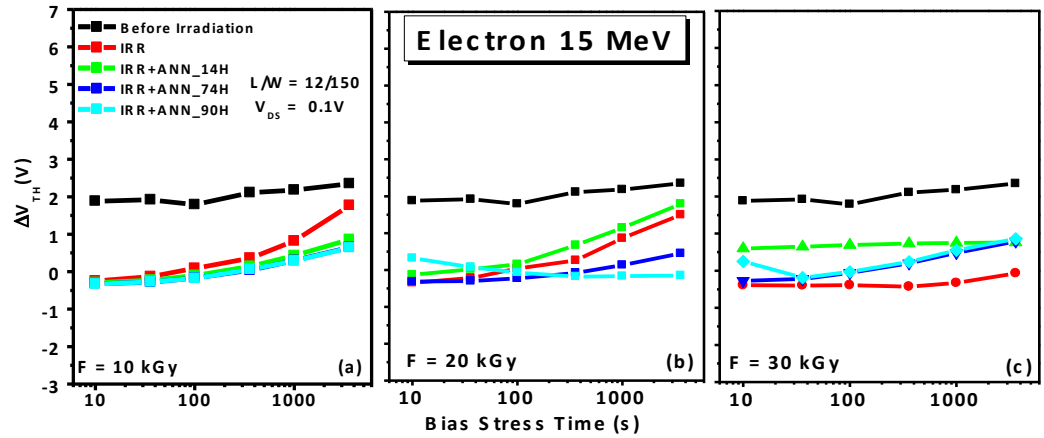

Fig 4.6. The threshold voltage hysteresis time evolution for 15 MeV electron irradiated MOSFETS#1 at 10 kGy (a), 20 kGy (b) and 30 kGy (c) after irradiation and several time annealing (14h, 74h and 154h).

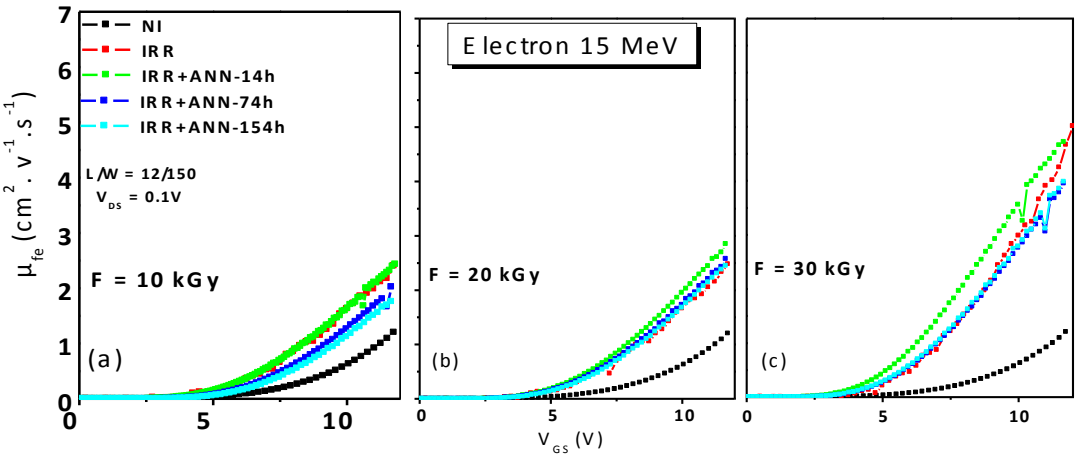

Fig 4.7. The field effect mobility time evolution after a NBS for 15 MeV electron irradiated MOSFETS#1 at 10kGy (a), 20 kGy (b) and 30 kGy (c) after irradiation and several time annealing (14h, 74h and 154h).

after a long time annealing is pretty similar to that of the post-irradiation, as shown in [Fig 4.7. a, b, c and d]. The values obtained during the first ramp up before the 10s stress are summarized in [Table 4.3]. Moreover, it can be seen from this table that V_{oxide_br} is not impacted by irradiation, confirming that V_{oxide_br} of a 4H-SiC MOSFET having a N_2O gate oxide is not impacted neither by the particle type (electron or proton), the fluence, the annealing time (at temperature up to 120ºC), nor by BSI stress. $I_{D\_SAT\_MAX}$ at V_{GS}=12V, shown coherent values regarding the variation of μ_{fe} and V_{TH} for all the electron doses, except in the case of the irradiation at 1kGy, that still remain under understanding.

High temperature operation behaviour

Due to its very peculiar behavior at high temperature, results of MOSFETs irradiated at 1 kGy are also presented. The V_{TH} variation with the operation temperature of all PIA MOSFET [Fig 4.8] seemed to follow the same trend as the one globally observed in the case of proton irradiation (see section 3.4.4). Unexpected results concern μ_{fe} behavior of PIA MOSFETs under temperature stress. Two different behaviors have been observed. The first one only occurs for the 15 MeV electron irradiation at an absorbed dose of 1 kGy [Fig 4.8.b]. In this case, we have extracted a μ_{fe} peak of 120 $cm^2.V^{-1}.s^{-1}$ when MOSFETs are operating at 250ºC [Fig 4.9.b].
Even at V_{GS} = 15V, μ_{fe} obtained is 60% higher than that of NI MOSFETs [Fig 4.9.a]. This is a very peculiar result since in all other PIA irradiation processes, μ_{fe} has practically the same value at high temperature. In addition, it is reminded that the obtained results are repeatable in the sense that, as in all the other cases, they have been measured on 4 MOSFETs#1 irradiated at 1kGy with similar electrical properties before and after irradiation.

The very high value of μ_{fe} observed at low gate voltage lead us to conclude that 1kGy irradiation should have lead, at high temperature to interfacial counter doping [3]. Indeed, surface counter doping refers, with surface counter doping, to doping the surface of the MOSFET p-body with n-type dopants. The main difference between interfacial and surface counter doping resides in the channel depth of the dopant consequently leading to the distinct transport mechanism. Surface counter doping lead to buried channels that are typically hundreds of nm deep into the semiconductor substrate, and the resulting mobility can be high at low field since transport of bulk carriers does not involve scattering from the interface [4]. More information about surface counter doping is given in section 5.2.1. In contrast, the interfacial counter doping depth is smaller, typically tens of nm or less. As a consequence, the scattering effect should be very high, hence, the drastic decrease of the μ_{fe} observed with the increase of the gate voltage once the μ_{fe} peak is reached.

The second remark is that at high temperature μ_{fe}'s PIA MOSFETs irradiated with an electron dose from 10kGy to 30 kGy with respect to NI samples is very similar and is illustrated with the case of 20kGy [Fig 4.9.c]. This behavior has also observed for 10 kGy and 30kGy.

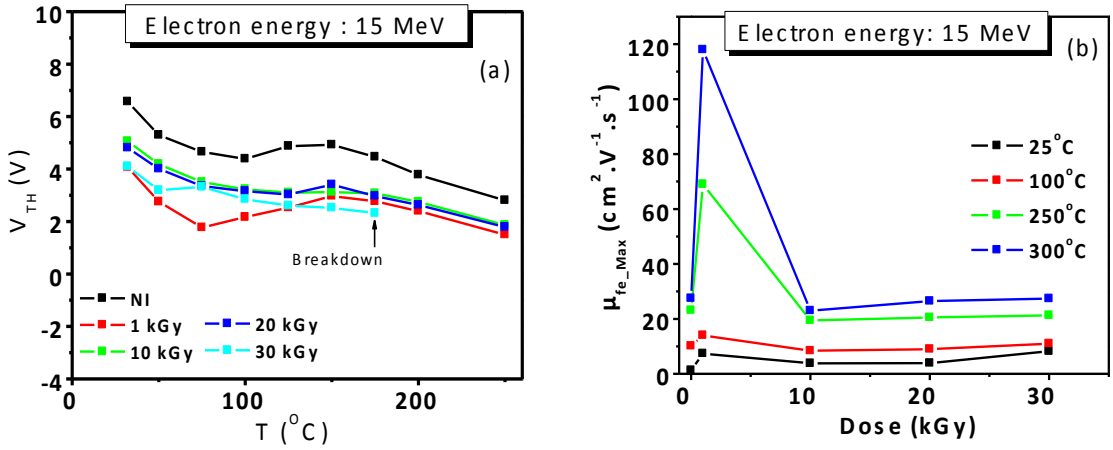

Fig 4.8. (a) The V_{TH} temperature evolution for the NI MOSFETs and PIA MOSFETs for all electron doses at 15 MeV electron irradiation and (b) the μ_{fe_Max} evolution with the increase of the dose for low, medium and high temperature.

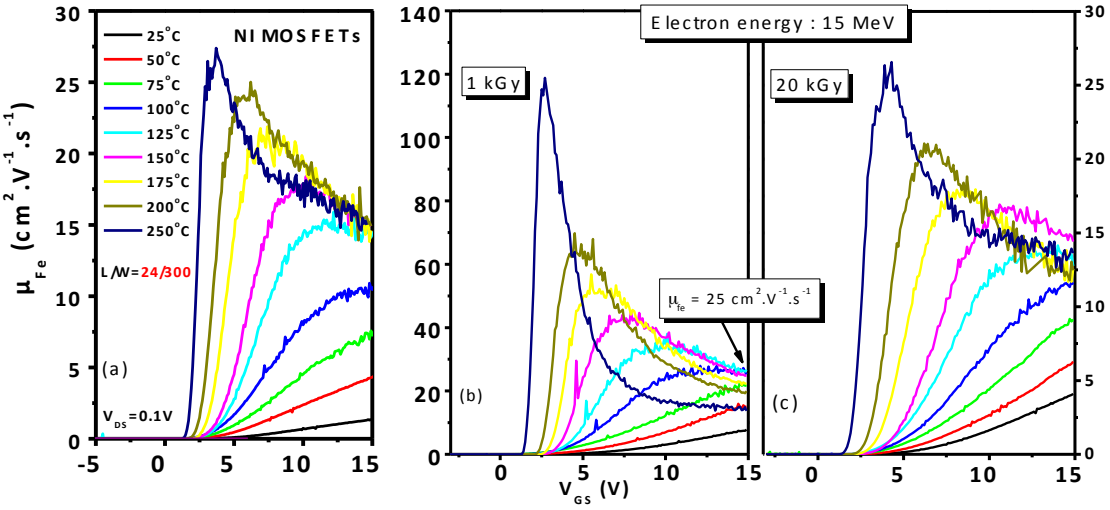

Fig 4.9. Evolution of the effective channel mobility with the increase of temperature for non-irradiated (a) and PIA MOSFETs irradiated at 15 MeV with an electron fluence of 1kGy (b) and 20kGy (c).

4.2.3. Charge build-up and recovery mechanism induced by electron radiation

The charge build-up mechanism that occurs during the electron irradiation process is similar to that of proton irradiation (see section 3.3.1 and 3.4.5). After electron irradiation, it is observed that V_{TH} is more stable and show a smaller negative shift under BSI for higher absorbed doses. For the lowest dose (1kGy) the initial ΔV_{TH} variation is lower than the NI MOSFETs. When electrons are injected in the device, especially into the oxide layer, the positive charges already present before the irradiation get neutralized, and hence stop acting as trapping centers. Therefore, a reduction of active traps at the interface may justify the μ_{fe} increase. A Nitrogen diffusion might also occur as described in section 3.4.5. According to the literature, in Si devices, ΔV_{TH} increases in amplitude at high electron doses [5], whereas in our

case the ΔV_{TH} variation not only decreases but also shows acceptable time stability (excluding the 1kGy case). In addition, it has been demonstrated that electron irradiation on SiC material clearly induced the creation of deep level defects [6-9] that might induce strong V_{TH} instabilities, which are clearly detected after the PIA process.

PIA behavior of electron irradiated MOSFET is similar to that of section 3.4.6. However, hydrogen atom formation inside the epilayer is impossible, and case 4 (of section 3.4.6) has to be ignored. Nevertheless, the other phenomena have to be considered. The amount of free electron (coming from irradiation) moving during the annealing and which may fall into acceptor traps at the SiO_2/SiC interface, can be higher than the amount of generated holes that, during the annealing process fall into donor traps. However, it does not prevent the holes to induce V_{TH} instabilities, especially due to its very low transportation process.

4.2.4 Conclusion on irradiated and annealed MOSFETs with N2O gate oxide

Irradiation process with a high electron irradiation energy: It has been evidenced that, the higher the absorbed dose, the lower V_{TH}, the more stable V_{TH_NBSI} and ΔV_{TH} with time, but also the higher μ_{fe}. We have assumed that this particle interact quite similarly to the proton one, with the exception that it can introduce a negative charge either inside the oxide or in the epilayer, inducing an enhancement of the V_{TH} negative drift.

PIA Process: After annealing, results have shown that, even if the V_{TH} instability is slightly corrected for all case, ΔV_{TH} increase is generally worse after irradiation for all doses and after the PIA when compared to that of the NI MOSFET. Moreover, μ_{fe} is not really impacted by the PIA process.

The case of irradiation at 1kGy is not very well understood. For this dose, a very high μ_{fe} peak has been observed, and it is the only case where its values at V_{GS}>12V and at T=175ºC are superior to that of the NI MOSFETs, by 60%. To justify such a behavior, we suspected that irradiation also generated interfacial counter doping that activated only at 250ºC. For all the other absorbed doses, μ_{fe} of PIA MOSFETs remained similar to that of the NI MOSFETs.

4.3. High-Energy Electron Irradiated MOSFET having a N_2O + TEOS Gate oxide

We have irradiated MOSFET#2 type (N2O+ TEOS) with electron 15 MeV.

4.3.1. Global analysis

Effect of radiation dose on the transconductance

The results shown that the electrical behavior of MOSFETs irradiated under electron beam have a very clear trend. The transconductance shifts toward negative values when increasing the irradiation dose. As in the previous section, the I_{DS} (V_{GS}) drift of the irradiated at

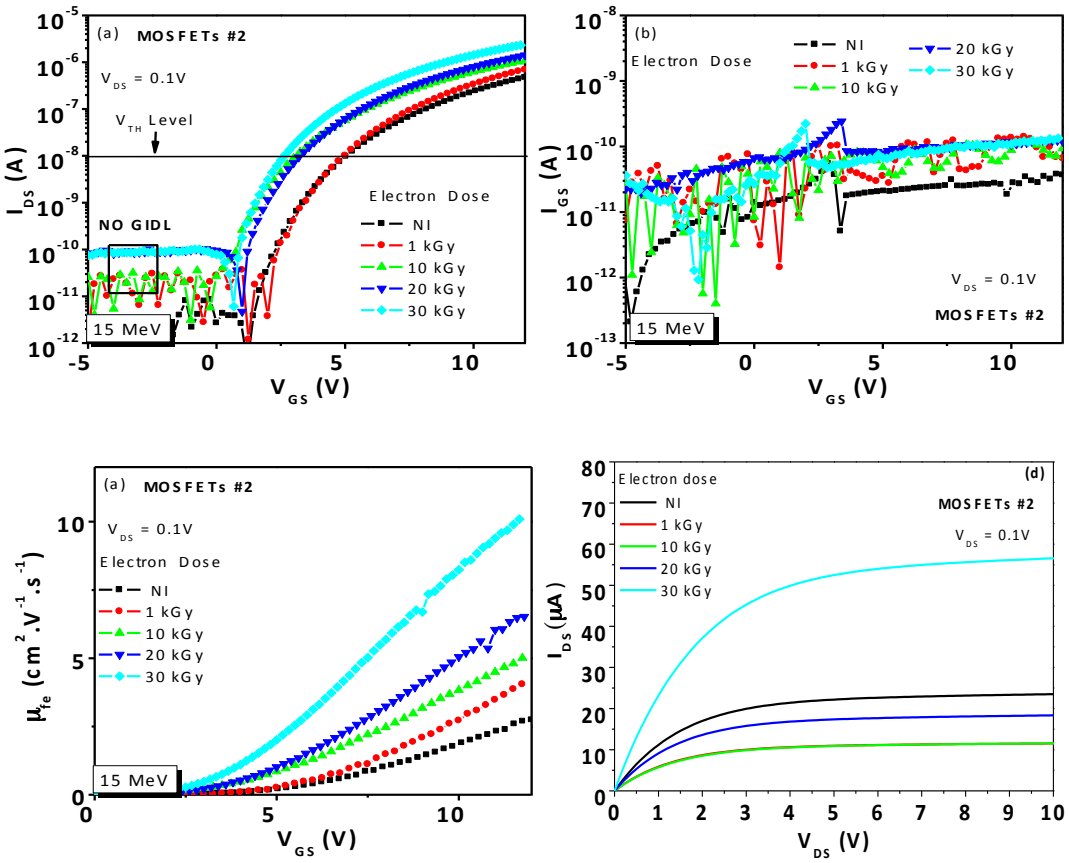

Fig 4.10. **Electrical characteristics of 15 MeV electron-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) I_{DS} (V_{GS}) at V_{DS} = 0.1 V (a), I_{GS} (V_{GS}) (b), μ_{fe} (V_{GS}) (c) and I_{DS} (V_{DS}) at V_{GS} = 12V (d).**

30 kGy and the NI MOSFETs#2 are equal despite of the thinner oxide transition layer compare to MOSFETs#1 [Fig 4.10.a]. In all the cases, neither GIDL current nor gate leakage current [Fig 4.10.b] has been detected. Then, contrary to section 4.2, the higher the electron absorbed dose, the higher the μ_{fe} [Fig 4.10.c], indicating in this case the higher oxide quality in comparison with MOSFETs#1: No single event has been observed at 1 kGy. Finally, apart from the irradiated MOSFETs at 30 kGy, the drain current capability has decreased in comparison with the NI values [Fig 4.10.d].

BSI Stress

The BSI measurement revealed the main weakness of high electron energy irradiated gate oxide, which is its poor V_{TH} stability. Indeed, compared to MOSFETs#1 (see section 4.2), the electron irradiation in MOSFETs#2 shown a no negligible V_{TH} instability. Contrarily to section 4.2, the higher the absorbed dose, the worse the V_{TH_NBSI} and ΔV_{TH} stability as shown in [Fig 4.11.a and b]. This behavior suggests a higher amount of oxide and interface charge traps introduced during the BSI process. It is reminded that the N_{it} + N_{ox} values shown in table 4.4 correspond to the first value extracted after the first step of BSI process (t=10 s). Furthermore, at 30kGy, acceptors trap charges at or near the SiO_2/SiC interface are increasing with the BSI time.

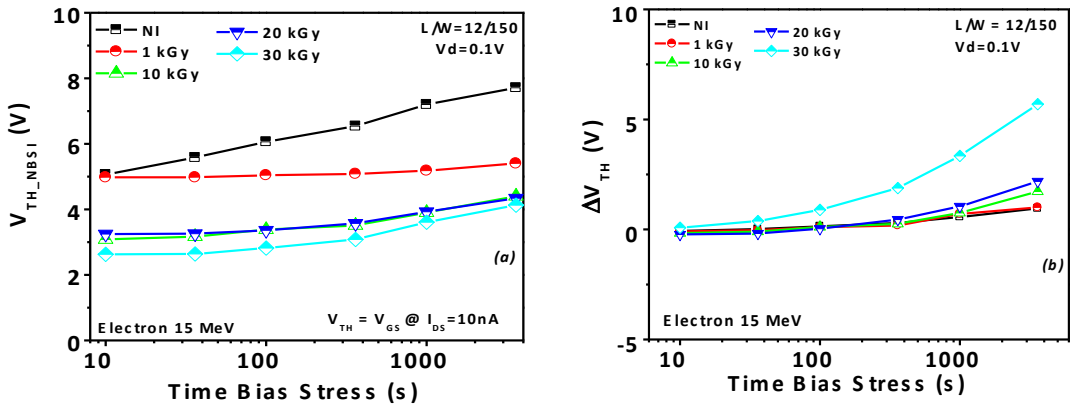

Fig 4.11. **Electrical characteristics of 15 MeV electron-irradiated 4H-SiC MOSFETs (L = 12 µm and W = 150 µm) V_{TH_NBSI} = f (t) at V_{ds} = 0.1 V (a), ΔV_{TH} = f(t) (b) and μ_{fe} (V_{GS}) (c).**

Other Parameters

In our measurements a slight decrease of the V_{oxide_br} is observed (table 4.4), but its decrease is lower than 5% in the worst case. Thus, we cannot consider the irradiation has a negative impact on the oxide breakdown voltage. Even if the main electrical parameters have been improved under electron irradiation, a critical problem of threshold voltage stability persists and, especially, on the electron-irradiated MOSFETs at the highest dose. Thus, from EP stability point of view, and despite of current capability and μ_{fe} increase, the electron irradiation didn't produce any real improvement of the global device performances. Hence a study based on the post-irradiation annealing to study possible recovery effects is needed.

Electrical Parameters	Non Irradiated	Electron Energy: 15 MeV			
		1 kGy (Si)	10 kGy (Si)	20 kGy (Si)	30 kGy (Si)
$V_{TH\_NBSI\_t=10s}$ (V)	5.06	4.98	3.08	3.24	2.63
V_{oxide_br} (V)	47.2	46.5	46.5	45.1	45.2
$\mu_{fe\_Vg=12V}$ ($cm^{-2}.V^{-1}s^{-1}$)	2.7	4.14	5.12	6.66	10.34
$I_{D\_SAT\_MAX}$ (µA)	23.23	11.42	11.14	18.54	56.14
$\lvert N_{it} + N_{ox} \times 10^{12} \rvert$ (cm^{-2})	0.040	0.051	0.096	0.034	0.039

Table 4.4. 4H-SiC MOSFET main electrical parameters before and after 15 MeV electron radiations at four different absorbed doses.

4.3.2. Bias Temperature Instability Impact

Time annealing impact

The PIA process allowed observing V_{TH_NBSI} instabilities of electron irradiated MOSFETs#2 at all doses, as shown in Fig 4.12.a, b, c and d. V_{TH_NBSI} Instabilities observed are

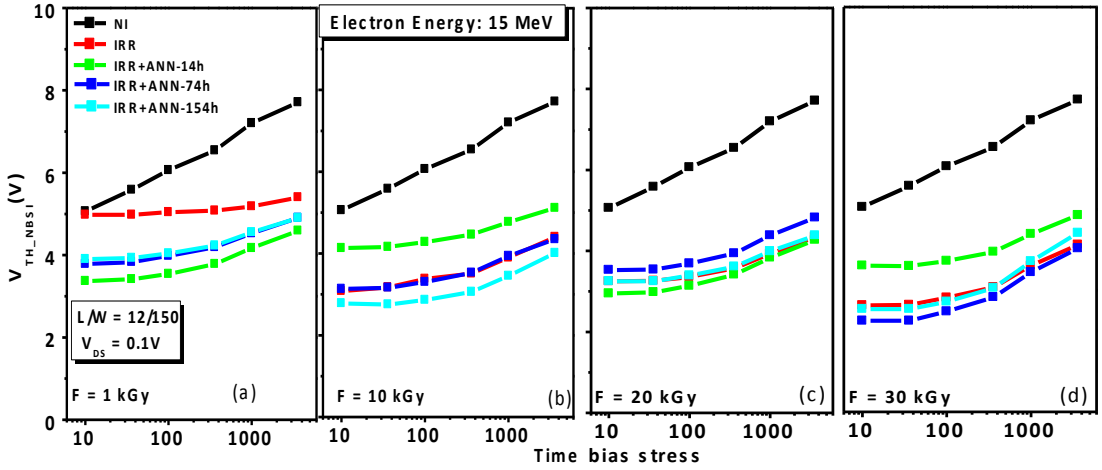

Fig 4.12. The threshold voltage time evolution after a NBS for 15 MeV electron irradiated MOSFETS#2 at 1 kGy (a), 10 kGy (b), 20 kGy and 30 kGy (d) after irradiation and several annealing time (14h, 74h and 154h).

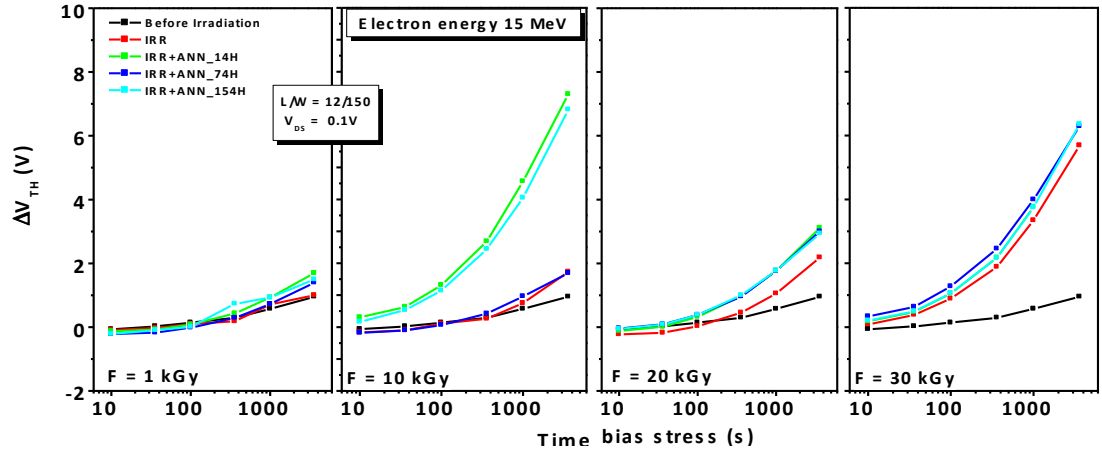

Fig 4.13. ΔV_{TH} time evolution after a NBS for 15 MeV electron irradiated MOSFETS#2 at 1 kGy (a), 10 kGy (b), 20 kGy and 30 kGy (d) after irradiation and several annealing time (14h, 74h and 154h).

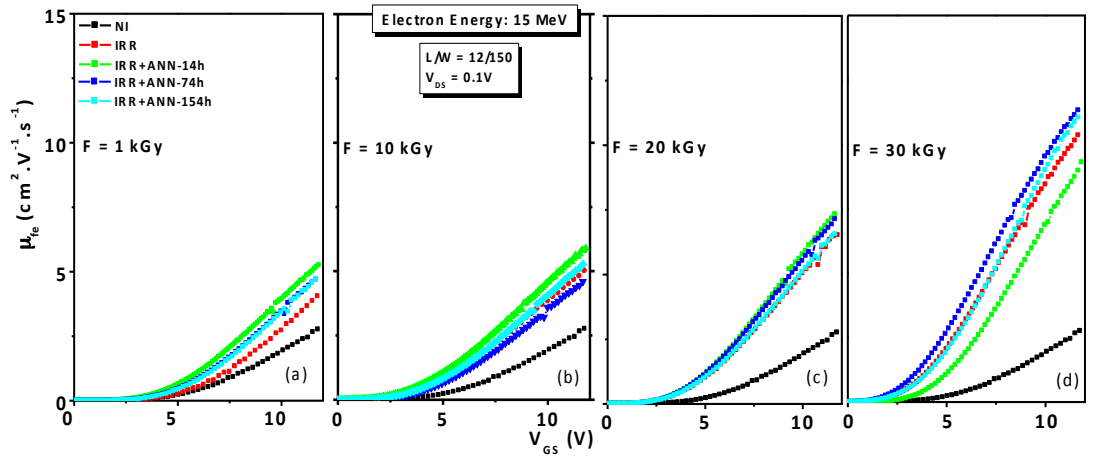

Fig 4.14. The field effect mobility time evolution after a NBS for 15 MeV electron irradiated MOSFETS#2 at 1 kGy (a), 10 kGy (b), 20 kGy and 30 kGy (d) after irradiation and several annealing time (14h, 74h and 154h).

15 MeV Electron absorbed dose (kGy)	NI	1		10		20		30	
		IRR	ANN	IRR	ANN	IRR	ANN	IRR	ANN
$V_{TH\_NBSI\ t=10s}$ (V)	5.06	4.98	3.90	3.08	2.78	3.24	3.25	2.63	2.54
V_{oxide_br} (V)	47.2	46.5	46.3	46.5	45.9	45.1	45.5	45.2	44.4
μ_{fe} ($cm^2.V^{-1}s^{-1}$)	2.7	4.14	4.68	5.12	5.27	6.66	6.55	10.34	11.02
$I_{D\ SAT\ MAX}$ (µA)	23.23	11.42	19.41	11.14	14.4	18.54	16.1	56.14	54.4
$\lvert N_{ox} + N_{it} \rvert$ x 10^{12} cm^{-2}	0.040	0.051	0.060	0.096	0.040	0.034	0.020	0.039	0.050

Table 4.5. The extracted electrical parameters on irradiated at 15 MeV proton energy for different doses, and PIA 4H-SiC MOSFETs#2.

worse than that observed in the case of PIA study of MOSFETs#1. At F = 1kGy and 10 kGy, the V_{TH_NBSI} values globally decreased after the PIA process of MOSFETs#2. In these cases, the PIA process is suggested having provoked charge detrapping that might increase the amount of donor-like traps at the SiO_2/SiC interface, inducing a V_{TH_NBSI} decrease. This V_{TH_NBSI} variation didn't changed with longer time PIA on MOSFETs irradiated at F = 20 kGy and 30 kGy compared with their value before the PIA process. Then, the ΔV_{TH} variation after the MOSFET irradiation process appeared to be critical, but it gets worse after the PIA process. The only case where ΔV_{TH} variation is not so unstable (in comparison with the NI MOSFETs) is when the PIA process is applied to the MOSFETs irradiated at F=1kGy [Fig 4.13.a]. When F > 1kGy, the ΔV_{TH} amplitude after annealing increases (> 3V). Concretely, the additional $\lvert N_{ox} + N_{it} \rvert$ charges being involved after the longest stress time were higher than $3.8 \cdot 10^{12}$ cm^{-2}, $1.6 \cdot 10^{12}$ cm^{-2} and $3.6 \cdot 10^{12}$ cm^{-2} in the case of the MOSFETs irradiated at 10kGy, 20kGy and 30kGy, respectively [Fig 4.13.a, b, c]. The μ_{fe} of the MOSFET#2 after PIA did not shown any significant variation for irradiated samples up to 20kGy [Fig 4.14.a, b and c]. The μ_{fe} of MOSFETs irradiated at F = 30 kGy show a slight increase after a long PIA, meaning that, in addition to the hole effect at the SiO_2/SiC interface inducing V_{TH} instability, N-diffusion phenomena may also occur during the PIA process. The main values of the MOSFETs#2 electrical parameters can be founded in Table 4.5. The oxide breakdown voltage didn't show any changes for all MOSFETs after PIA. The thicker gate oxide of MOSFETs#2 does not seem to increase the robustness, especially at high irradiation energy. Hence, proton irradiation seems to be preferable from this point of view to electron irradiation for MOSFETs improvement.

Temperature operation impact

When increasing the operation temperature, the V_{TH} curious behaviour observed in all the previous cases of PIA MOSFET#2 irradiated with protons (see section 3.5.4) also occurs under electron irradiation [Fig 4.15.a]. In addition, Electron irradiation of PIA MOSFETs#2 irradiated at 1, and 10 kGy shown similar behaviour of μ_{fe} [Fig 4.15.b]. Beside, a very high μ_{fe} peak (>250 $cm^2.V^{-1}.s^{-1}$) has been also observed at 250ºC in the case of F= 20kGy [Fig 4.15.b] and F = 30kGy [Fig 4.16.c]. However, at high electric field (V_{GS} > 12V), μ_{fe} value strongly decrease and remain similar to that of the PIA MOSFETs irradiated at F=1 and10 (results for 1 and 20kGy are not shown in the figure). The resulting values are pretty much equal to that of

the NI MOSFETs [Fig 4.16.a]. In all the cases, the gate leakage current of all the irradiated and post-annealed MOSFETs is not higher than the NI case, remaining below 2 nA at 250°C at V_{GS}=15V.

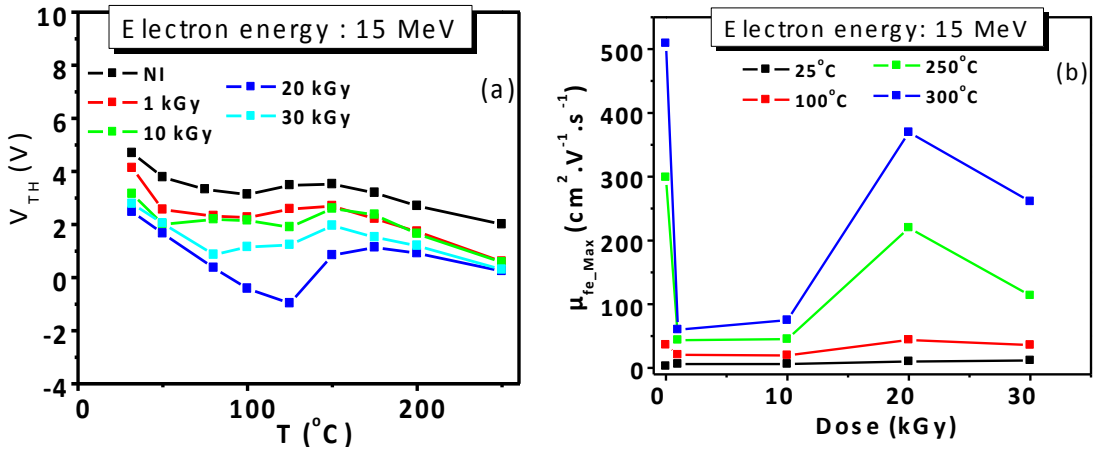

Fig 4.15. The V_{TH} temperature evolution for the NI MOSFETs and PIA MOSFETs of all fluences and doses at a electron irradiation of 15 MeV for all absorbed doses. and (b) the μ_{fe_Max} evolution with the increase of the dose for low, medium and high temperature.

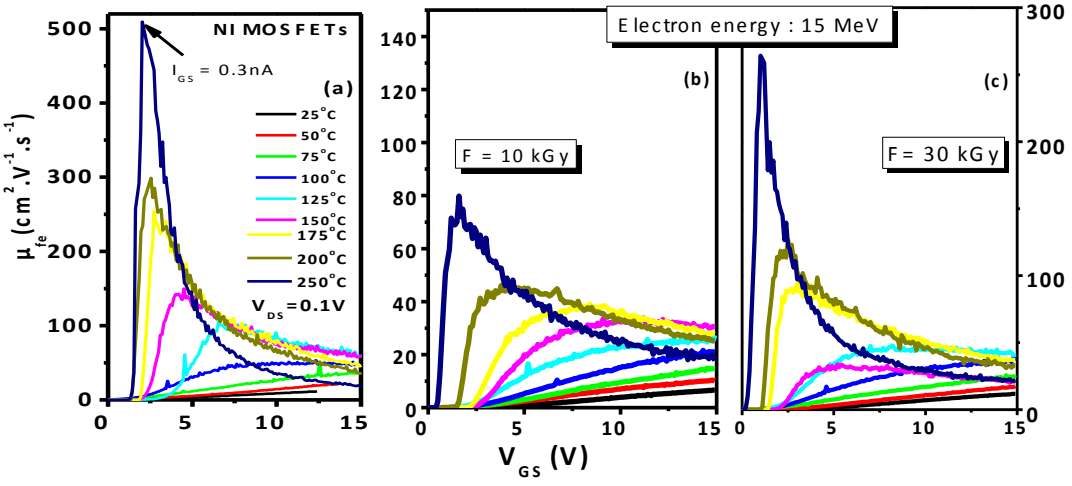

Fig 4.16. Evolution of the effective channel mobility with the increase of temperature for non-irradiated (a) and PIA MOSFETs irradiated at 15 MeV with an electron dose of 10 kGy (b) and 30 kGy (c)

4.3.3 Conclusion on post irradiation annealed MOSFETs with N_2O + TEOS gate oxide.

Post-irradiation annealing performed on MOSFET#2 having N_2O+TEOS gate oxide has shown serious threshold voltage hysteresis instability issues. These issues are not very well understood, and they seem to occur at random irradiated doses. The experiments evidence that, the probable cause of the observed V_{TH} instability is related either to the oxide thickness or to the amount of generated interface charges within the interface transition layer. It is suggested

that, with a thick oxide, the amount of e-h pairs generated by irradiation is superior to the ones generated in a thin oxide. Thus, instabilities due to charge issues can occur with much probability and might be enhanced by the post irradiation annealing process. A positive aspect of N_2O + TEOS gate oxide configuration (MOSFETs#2) is that the interface roughness at high temperature annealing, in some cases, has been improved, and, contrary to MOSFET#1, has shown a much better μ_{fe} at high V_{GS}. More positively, there is no detection of any kind of leakage. Moreover, the oxide breakdown voltage remained equal for all the irradiated and non-irradiated devices.

High electron irradiation energies : Despite of the continuous μ_{fe} increase, and of the small V_{TH} decrease with the irradiation absorbed dose, the critical V_{TH} stability issues do not allow concluding about real positive effects of the electron irradiation at high energies on the MOSFETs EP. The obtained results indicate that irradiated MOSFETs#1 having a thinner gate oxide are less sensible to high electron irradiation energies.

PIA Process: The PIA process induced both V_{TH_NBSI} and ΔV_{TH} instability for all irradiation dose. The obtained instability is worse than the one observed in the case of the PIA study on MOSFETs#1. The μ_{fe} didn't seem to change: Its values remained the same before and after the PIA process. Also in this case, the high temperature stress induced two turnovers of the V_{TH}: The V_{TH} initially starts to decrease with the temperature increase in the range of [25ºC; 125ºC], then increases in the range [125ºC ; 175ºC] before decreasing again in the range of [175ºC ; 250ºC]. The μ_{fe} at high temperature has shown two types of behavior: One regarding the 20 and 30 kGy irradiated MOSFETs MOSFETs annealed at 120ºC, and another one regarding the PIA MOSFETs at irradiation doses of 1 and 10 kGy. In both cases, the high field μ_{fe} value at T=250ºC and V_{GS} > 12V are the same as the one of the NI MOSFETs.

4.4. General conclusion

In a first time, 4H-SiC MOSFETs with an oxynitrided gate oxide have globally shown an electron irradiation robustness behavior for irradiated doses up to 30 kGy. Field effect mobility also increased. However, this behavior might not be exclusively related to the nitrogen diffusion but also, to the neutralization of the positive charges present before irradiation. The observed V_{TH} instability could be due to deep defect generated either at the SiO_2/SiC interface or within the epilayer. In addition, the temperature annealing does not produce any changes of μ_{fe}'s PIA MOSFETs at high gate voltage operation (>12V), accounting for the roughness predominance on the other effect. Nevertheless, it has been seen that the annealing process induced critical instabilities, accounting for a predominance of the positive charges that are brought at the SiO_2/SiC interface during the BSI stress. These important instabilities shown that electron irradiation does not guarantee a proper operation of 4H-SiC MOSFET.

4.5. References

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Section 3

A New Fabrication Process Approach

Chapter 5
An Optimized Gate Oxide Process

Up to now, all the experiments have been performed on 4H-SiC MOSFETs having a standard poor SiO_2/SiC interface quality. In this chapter, a way to improve the gate oxide process has been investigated. The new gate oxide process is proposed and experimented. With this improved gate oxide, 8º OFF axis epilayer MOSFETs, 8º OFF axis implanted MOSFETs and ON Axis MOSFETs are fabricated. Electrical properties are extracted from the electrical characterization.

5.1 Modified Gate Oxide Processes

We basically started from an initial oxidation process presented below in this section. The reasons for choosing such initial process are pointed out and their main electrical characteristics are shown. The best oxidation process is selected for MOSFET fabrication and the results are compared with those from the starting process. Note that, the experiment performed in the frame of this chapter account for a further evaluation of the irradiation impact on MOSFETs with a better interface quality than that shown in the previous chapters.

5.1.1 Oxidation Process: Starting Point

The last advanced oxidation process designed at CNM in 2011 [1] has been considered as a starting point, and the main effort carried out in this chapter has been focused on improving this process. The main objective was to reduce the interface states density and increase effective channel mobility while keeping the threshold voltage stable with time and temperature stress. This starting oxidation process is different from the previous ones studied in chapter 3 (MOSFETs#1 and MOSFETs#2) due to the fact that in that cases it was important to study the irradiation impact on n-channel MOSFETs having a low SiO_2/SiC quality in order to better put in evidence the irradiation and annealing effects. The process is performed on a 4H-SiC Si-face 8º off-axis p-type epilayer with a doping concentration of $5 \cdot 10^{16}$ cm^{-3}. After a RCA cleaning, the sample is loaded into a RTP furnace for oxidation. In [Fig.5.1.a], the RTP temperature profile sequence used for this reference oxide is given. Prior oxidation, a surface pre-treatment consisting in an *in-situ* RTA step was carried out in H_2 at 800ºC for 2 min (as in MOSFETs#2 in chapter 3). Then, the oxide is grown by RTO in 100% N_2O at 1050°C for 10 min, resulting in an average oxide thickness of 42.5 nm. Finally, a post-oxidation annealing in Argon is performed during temperature ramp down.

In her previous work [2-5], A. Constant highlighted the critical relevance of H_2 RTA pre-oxidation step (see chapter 1). RTP *in situ* H_2 allows reducing the native oxide and metal contaminant present at the wafer surface. Thus, the density of surface defect is reduced. Once

the surface is properly hydrogenated, there are less available initial defects able to be oxidized. On [Fig.5.2.a], we can see a comparison of normalized capacitance C-V curves of a MOS capacitance with and without H_2 RTA. For a RTA N_2O oxidation (Sample #1) there is a shift in the C-V curves between the first and the following measurement (t1, t2) due to slow traps in the oxide. This indicates the presence of ion mobile charges, oxide charges and deep interface states trapping event with long response time [1]. These effects are not found after H_2-RTA (sample #2 in ref [1]).

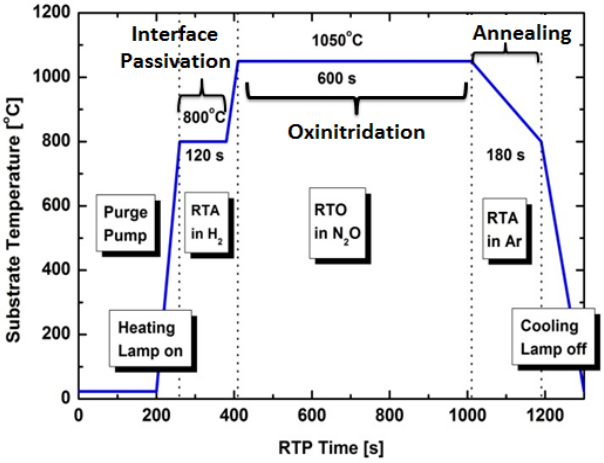
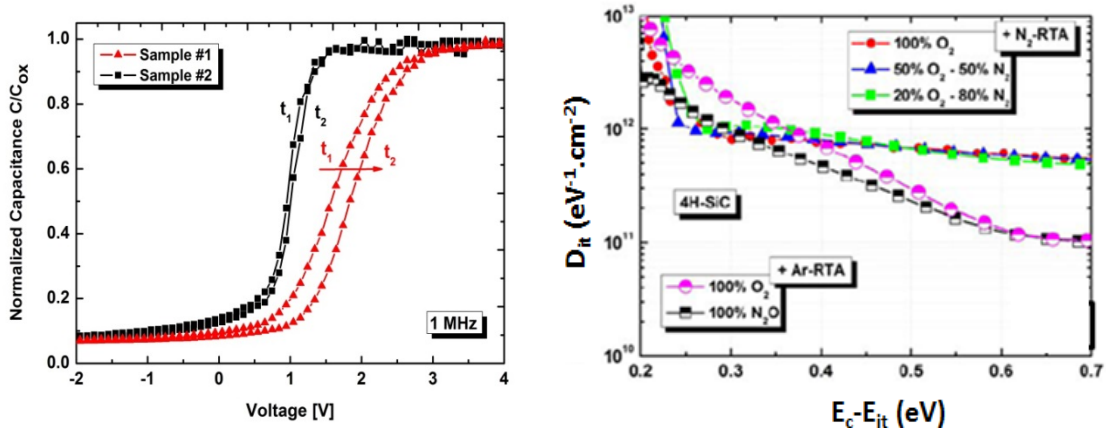


Fig.5.1. RTP Sequence used in the last experiment, combining three successive steps.

On the other hand, as it can be inferred from [Fig.5.2.a], among many oxidation processes used in our previous works, N_2O RTO [1050ºC, 600s] followed by an Argon RTA is the one whose D_{it} above the conduction band shows the lowest values. The extracted D_{it} values are relatively low (values between 3.10^{12} and 10^{11} $eV^{-1}.cm^{-2}$). Therefore, this process introduces the main objective of this thesis, which is to improve the 4H-SiC MOSFETs performances by acting on the oxidation process step. In order to accomplish this goal, an optimum trade-off between time, temperature and gas molecules used before during and after oxidation is required. Although the



(a) (b)

Fig.5.2. MOS capacitance C-V characteristics with hysteresis effect. The black and red curves represent the C(V) response of MOS capacitor having a grown dielectric with and without hydrogenation (a). Comparison of the interface state density (D_{it}) vs Energy, for oxides grown on 4H-SiC by the different RTO processes (b).

oxinitridation step is well mastered, it could be possible to modify it. Moreover some external additional parameters could also be taken into account, like for example a pre-cleaning step or a proton/electron irradiation step once the component is fabricated.

5.1.2 Gate Oxide Growth Process Modifications

The starting material for all the tested samples in this chapter is described in section 3.2.2. From the first experiment, four MOS capacitors have been fabricated based on a different gate oxide processes described in Fig.5.3.

1. The oxidation process starting point described in the previous section is used as a reference and shown in [Fig 5.3.a].

2. In the second sample [Fig.5.3.b], a $POCL_3$ annealing associated with a N_2O RTA oxidation (P2) has been tested. The reason of such a process is due to the excellent mobility result (μ_{fe} = 87cm^2. V^{-1} with L/W = 30/200 = µm under V_{DS} = 0.1V) associated with a very low interface density (D_{it} = 9 x 10^{10} cm^{-2}.eV^{-1} above the conduction band for an oxide layer on p-type SiC) obtained by D. Okamoto et al [6-7] while using a dry oxidation + $POCL_3$ anneal in a classical furnace. Subsequently, similar results were also reported by Sharma et al using SiP_2O_7 planar diffusion source (PDS) [8]. Important negative V_{TH} shift after a positive gate bias at high temperature have been observed due to the fact that P_2O_5 converts the SiO_2 to PhosphoSilicate Glass (PSG), a polar material that introduces voltage instabilities which negate the benefits of lower D_{it} and higher μ_{fe}. The phosphorus treatments that passivate interface traps also result in interfacial counter doping [9] against conventional bulk counter doping, was used by Liu and al [10]. This stability problem has been solved by introducing a stack gate oxide structure consisting of a PSG layer (1nm) followed by a deposited oxide [11]. CNM do not dispose of P_2O_5 planar diffusion source. But it has been thought that, by performing a $POCl_3$ POA under RTP furnace after a N_2O gate oxide, additional information about $POCl_3$ impact on μ_{fe} and V_{TH} time stability could be founded.

3. The third process, described in [Fig 5.3.c], came directly from process [1] and implicates a longer Argon post-annealing step, allowing a better self-rearrangement of the crystal lattice after the oxidation: The longer the annealing time, the higher the oxide quality.

4. For the last process of [Fig.5.3.d], RTO-N_2O oxinitridation is replaced by three H_2-O_2 temperature pulses (P4). This process is the result of a meeting in the frame of the NetFISiC project, where it has been insisted on the high relevance effect of hydrogen over interface passivation. Thus, instead of making one oxidation layer of 45 nm thicknesses, it has been decided to split the layer into three sub-layer of 15 nm each,

and separate each process between two layers by an intermediate step consisting in a 800ºC hydrogen cleaning. In this way, it could have help decrease the dangling bond density and helped to passivate the carbons at the SiO_2/SiC interface.

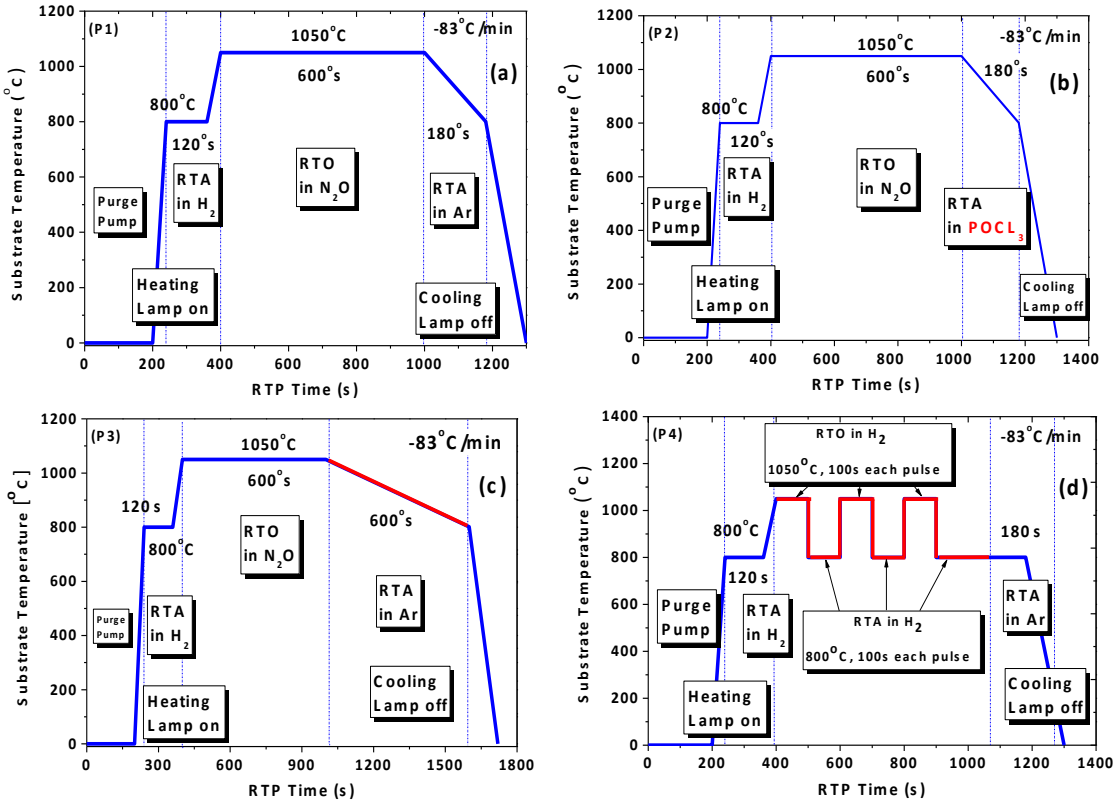


Fig.5.3. Reference gate oxidation process, with H_2 surface treatment, N_2O oxinitridation and Ar annealing (P1) (a), H_2-O_2 Pulse while RTP oxidation processing (P2) (b). RTP Oxidation gate oxide with a longer argon rapid thermal annealing (600s) (P3), RTP Oxidation gate oxide with a $POCl_3$ rapid thermal anneal (P4).

5.1.3 Comparative Study of Electrical Parameter from C (V) Curves

Typical C-V curves from MOS capacitances obtained with the 4 processes mentioned in the previous part are shown in [Fig.5.4.a]. The corresponding calculated interface state density above the valence band is shown in [Fig.5.4.b]. [Table.5.1] summarises the results on the four proposed experiments. Note that the theoretical flat band voltage V_{fb} for our p-type material has been founded to be -2.43V. The experimental V_{fb} increases drastically with the $POCl_3$ process (>10V). It indicates that that $POCl_3$ cannot be used combined with RTO N_2O oxide, since a very large flatband voltage is synonym of a very high amount of effective oxide charges that will provoke V_{TH} instability during the time BSI measurement. In this case, N_{eff} is one order of magnitude higher than the reference sample, and N_{fc} is more than 3.5 times superior to the reference sample. This mean that, in addition to a very negative V_{FB}, the hysteresis flatband voltage ΔV_{FB} is also much larger than the one observed in the reference sample analysis. In addition, its D_{it} variation above the valence band is also higher than the ones observed in the other samples. The most remarkable results come from the 10 min Argon annealing process

Process	T_{OX} [nm]	V_{fb} [V]	N_{eff} [$\times 10^{11}.cm^{-2}$]	N_{fc} [$\times 10^{9}.cm^{-2}$]
P1 (standard)	48.40	-4.20	7.70	4.00
P2 (POCl3)	39.56	-12.56	75.35	14.71
P3 (Ar_10min)	43.10	-3.52	5.14	1.79
P4 (H_2_O_2)	43.20	-3.90	7.01	2.94

Table.5.1. Resume of the main electrical parameter extracted from C(V) curves. T_{ox} is the oxide thickness, V_{fb} the flatband voltage and N_{eff} the number of effective oxide charge and N_{fc} the amount of fixed charges. Note that the theoretical V_{FB}, in our case has been founded to be -2.43V.

(P3). Indeed, among all the processes, (P3) is the one exhibiting the lowest defects density values: In comparison with all the other samples, the V_{fb} of (P3) is closer from the theoretical values, N_{eff} and N_{fc} are 25% and 40% lower than that of the (P4) process, respectively. Moreover, the D_{it} values are much lower than that of the other process. Thus, it confirms the hypothesis predicted previously on the Argon annealing benefits. In the case of the H_2-O_2 pulsed process (P4), it exhibits slightly lower flatband voltage values than the reference process (P1), and with a lower D_{it} in the E_{it}-E_v range of [0.2 eV; 0.4 eV]. Above 0.4 eV, the D_{it} is slightly superior to that of the (P1). The amount of N_{eff} of the (P4) process is lower that (P1) by 9% but it can be attributed to the fact that its oxide thickness is 11% lower as well. The N_{fc} observed together with the N_{eff} values indicates that the ΔV_{FB} of (P4) has also been reduced.

After this experiment and results of C(V) characterization, P3 was chosen as the best process for lateral MOSFET manufacturing due to its higher interface quality.

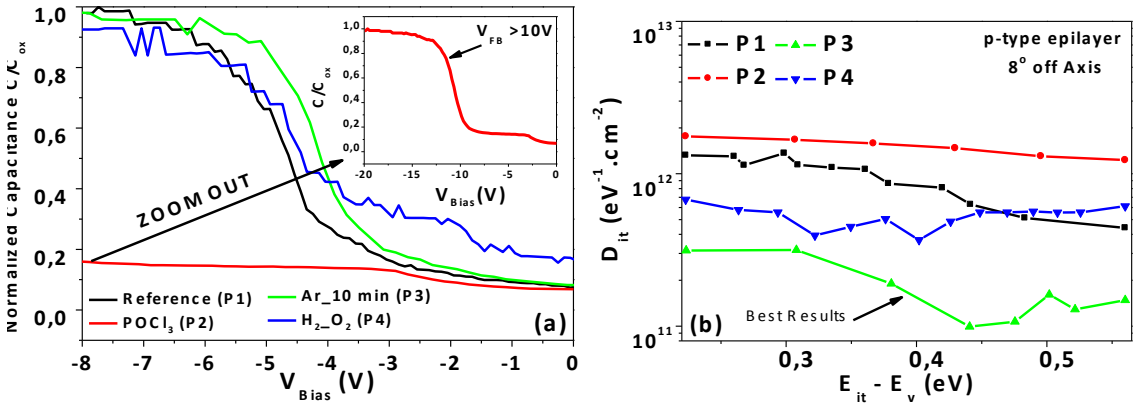


Fig.5.4. C(V) responses aspect of the four processes designed (a) and its respective D_{it} variation above the valance band (b).

5.1.4 MOSFET processing and electrical characterization

Wafer Processing

The starting material for MOSFET manufacture is a 4H-SiC Si-face 8° off angle substrate with a p-type epitaxy. For the gate oxide formation (P3) process has been used. After defining the drain-source contact windows, the ohmic contact had been formed by using a sputtering deposition of a Nickel layer (150nm) patterned by lift-off, and annealed in Argon at

950ºC for 2 minutes. For the sake of comparison, another sample was fabricated by using the starting reference process (P1) for gate oxidation.

Electrical characterisation

Electrical characterization has been carried out by using the time BSI and BTI measurement method. From the $I_{DS}(V_{GS})$ curves measured during this test [Fig.5.5 a and b], we can ifer that the V_{TH} instability seems to be slightly better in the case of P1, but the V_{TH} hysteresis is slightly reduced in the case of P3. The interface charge traps generated by the time BSI together with the electron charge trapping effect is not very relevant in the case of BSI analysis up to 3600s: The introduced $|N_{it} + N_{ox}|$ during the BSI is about $1.24 \times 10^{11}\ cm^{-2}$ in the case of the P1 process and is about $1.12 \times 10^{11} cm^{-2}$ in the case of P3, which is approximately equal from the ΔV_{TH} point of view. Unfortunately, from $I_{DS}(V_{GS})$ curves, it can be deduced that the Ar RTA has no effect neither on reducing the GIDL nor on the ion mobile charge decrease. An additional process might be required in order to reduce this additional increase of the off-state current after a positive bias stress. On the other hand, no gate leakage has been detected during the measurement. Moreover the oxide breakdown voltage has been founded to be around 35V for both processes, which is an acceptable value for lateral MOSFET devices [12].

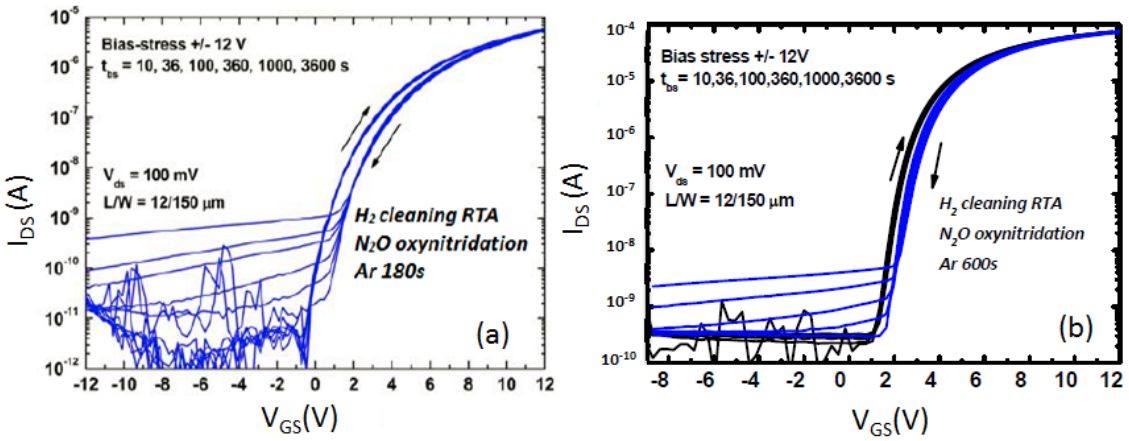


Fig.5.5. Evolution of the $I_{DS}(V_{GS})$ parameters while BSI measurement of the P1 process (a) and of the P3 process (b).

MOSFET channel mobilities

Corresponding Field effect mobility are extracted from $I_{DS}(V_{GS})$ and shown in [Fig 5.6.a] and [Fig 5.6.b]. The low amount of D_{it} extracted from the P3 MOS Capacitances [Fig. 5.4] is confirmed by the P3 MOSFET μ_{fe} improvement observed at T=25ºC. Indeed, when compared with the P1 process, the maximum μ_{fe} value has been increased. Moreover, its values at V_{GS} > 12V is also higher. At V_{GS} > 12V and above 100ºC, μ_{fe} of the P3 process tends to lose between 9% and 27% of its peak value (μ_{fe_max}), whereas in the P1 process, it tends to lose between 27% and up to 50% of its maximum value. In addition, the mobility slope in the range of [μ_{fe_max} ; μ_{fe} at V_{GS}=14V] is less tilted than in the P1 sample. Therefore, the P3 process has a better surface roughness or present less scattering effects. Indeed, in the case of the MOSFETs using the P3

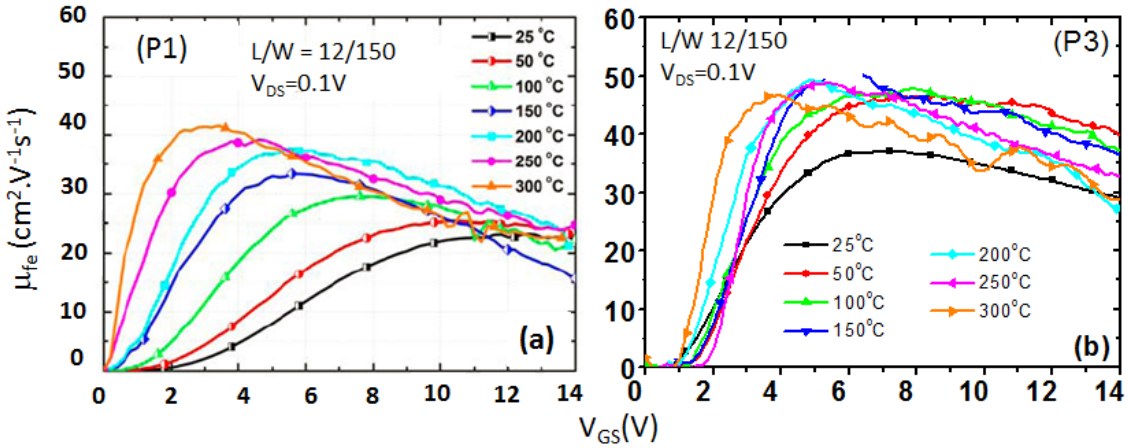


Fig.5.6 Evolution of μ_{fe} (V_{GS}) of the P1 (a) and P3 (b) oxidation process with the increase of temperature.

process, μ_{fe_max} starts to decrease with the temperature increase at 250ºC whereas it is not the case in the sample using the P1 process. This means that, the interface state density is low enough to allow the predominance of the phonon scattering effect. In the P1 process, it seems that 300ºC is not high enough to stop the predominance of the SiO_2/SiC interface charge scattering.

Temperature impact on V_{TH}

Low V_{TH} values are required for the consuming and control of the digital and power circuits currently developed at CNM [3]. However, these values do not have to approach 0V in order to keep the MOSFETs in the normally-off state. The variation of V_{TH} with the operation temperature is lower for the P3 process [Fig.5.14]. With the P1 process, there is an abrupt decrease of the threshold voltage in the temperature range of [25-100°C] whereas, in the case of the P3 process, this decrease is much less abrupt. Thus the risk of having normally-on devices at high temperature is lower with the P3 oxidation process.

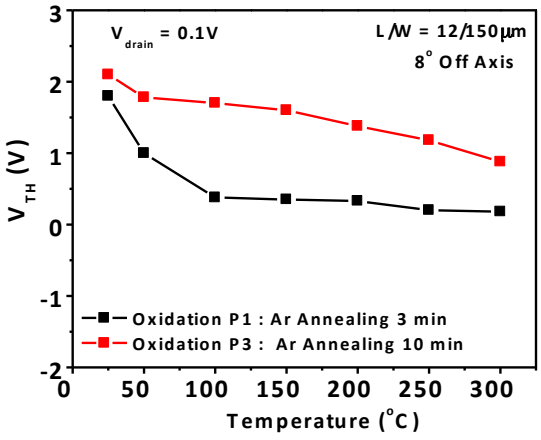


Fig.5.7. Evolution of V_{TH} with temperature for the two different oxidation process (P1) and (P3).

Conclusions

According to these results, it can be concluded that after the oxidation phase in N_2O, a larger annealing time in Ar time allowing the lattice recrystallization at high temperature, permit to reduce the D_{it}, to increase μ_{fe} and to improve the V_{TH} temperature stability while maintaining its time stability constant. However, the GIDL issue remains. This GIDL problem did not appeared in the case of MOSFETs#1 and MOSFETs#2 studied in chapter 3 and 4. To reduce this GIDL process, two possibilities are envisaged: Either a trade-off between hydrogenation temperature and N_2O oxidation process time need to be founded, or a way to improve the surface roughness of the epilayer might be necessary.

5.2 Novel Oxidation process of different substrates types

Once the gate oxidation process has been optimized, the GIDL current issue still remains. Thus, in order to deal with this problem while trying to improve further the interface quality, it has been decided to perform new experiments based on a modification of the starting substrate where the oxidation is performed. We proposed to study three types of starting SiC substrates: P-type epilayer structure 8º off-axis with phosphorus interfacial counter doping done by implantation, P-type layer doped with Aluminum implantation on 8º off-axis and on-axis structures.

5.2.1. Surface/interfacial counters doping

Liu and al explained that the nitrogen and phosphorus treatments that passivate interface traps result in interfacial counter-doping of SiC [13]. The concept of interfacial counter doping was used by Liu et al [14] to explain the high mobility of MOSFETs fabricated on the 11-20 face using phosphorus and nitrogen interface passivation. It was suggested that, in addition to passivating the interface defects, phosphorus diffuse a few nm into the SiC layer and act as active donors as well. This hypothesis was experimentally verified by Fiorenza et al [15]. Tuttle et al. also mentioned the same effect to explain the observed reduction of near interface traps in the presence of interfacial sodium, potassium, nitrogen and phosphorus. They show that the near interface trap energy levels are lowered by the impurities and thus become inaccessible to the experimental measurement [16]. The magnitude of the interface counter doping effect is still unknown. Thus, it might be interesting to proceed, in the frame of this thesis, to an additional phosphorus superficial implantation prior to oxidation and study the counter doping impact on the D_{it}, μ_{fe} and V_{TH} stability with time and temperature stress.

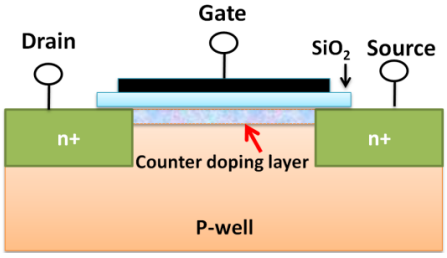


Fig 5.8. Cross section of an n-channel MOSFETs with interfacial counter doping layer (adapted from [9]).

5.2.2. On-Axis substrate: A primary difficulty in bulk growth

One of the breakthroughs in epitaxial growth of hexagonal SiC 30 years ago was the use of off-axis cut substrates in order to reduce the 3C inclusion at its minimum [17-20]. Since then, 8ºoff axis and more recently 4ºoff axis substrates were uses as standard for SiC devices fabrication. The impact of the off-axis nature of the interface on MOSFET performances was not extensively studied in the past. Our own experience and some literature papers tend to indicate that the lower the off axis angle, the better the MOS channel properties. For example in [21] K.Fukuda et al. concluded that the off-axis epitaxial angle below 1º could highly contribute to reduce the interface state density on C-face SiC, since it induces an improvement of surface roughness. However, no report based on the electrical behavior of a 4H Si-face MOSFET with on-axis orientation has been founded so far in the literature. This is probably due to the growth complexity of the process [22-23]. Indeed, in order to obtain an on-axis grown layer, the growth process needs to be carried out nearby the seed dislocations. Thus the lower the dislocation amount, the more difficult it is to grow. On the other hand, the higher the dislocation amount, the higher the leakage current [24-25] hence the difficulty to find and optimum compromise growth/dislocation.

We had the opportunity to access to best state of the art on-axis epitaxied 4H-SiC supplied by Anne Henry from Linkoping University. We have used this material to test the MOSFET performances on on-axis. We experimented and confirmed the efficiency of working with on-axis material by comparing several MOSFET samples having similar gate oxide but different angle-cut [*26-27*]. We will see that not only the on-axis angle can have an influence on the electrical parameter, but also, that the implantation dose can present very positives effects and can considerably decrease the threshold voltage value without switching the device normally-on. Atomic force microscopy (AFM) images [Fig.5.9.a] and signals [Fig.5.9.b] showing the roughness difference between on-axis and 8º off-axis sample are presented.

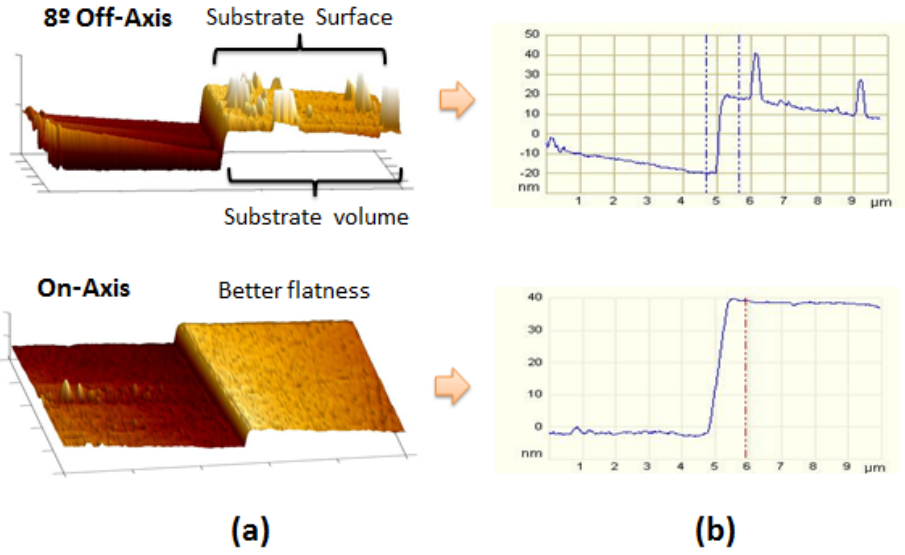


Fig 5.9. In (a) the AFM images of the 8° off-axis and on-axis sample, together with the associated AFM signal (b).

5.2.3. Samples definition and fabrication process

For this experiment, three sets of Si-face MOSFET samples have been fabricated.

1. Reference sample Epi (8º Off): built on a 10µm p-type epitaxial layer grown on 8º off-axis of n-type 4H-SiC substrate. The epilayer has an aluminum doping concentration of $5x10^{16}$ cm^{-3}. The SiO_2/SiC interface has been modified by surface counter doping using a 5 keV phosphorus with a dose of 6 x 10^{13} cm^{-2}. The implantation profile is shown in [Fig.5.10.a].

2. The second set of MOSFET, IMP (8º Off), is built on an 8ºoff-axis angle cut n-type substrate with a N-type epilayer doped at $5 \cdot 10^{15}$$cm^{-3}$. The wafer has been submitted to an Aluminum multi-implantation with a doping concentration profile shown in [Fig. 5.10.b].

3. The third set of MOSFET, IMP (ON), is built on the on-axis substrate mentioned in the introduction. An N-epilayer doped at $1 \cdot 10^{15}$ cm^{-3} has been grown in Linkoping University. Then, the wafer was Al implanted using the same implantation profile used for the second sample.

The photolithographic mask set consists in 7 levels including the alignment motives mask, the P-well implantation mask, the N+ implant mask for the source and drain definition, the gate active region definition, the contact openings and, the contact and gate metallization pattern. All the MOSFETs sets were oxidized with the P3 oxidation process defined in section 5.1.2 for gate formation.

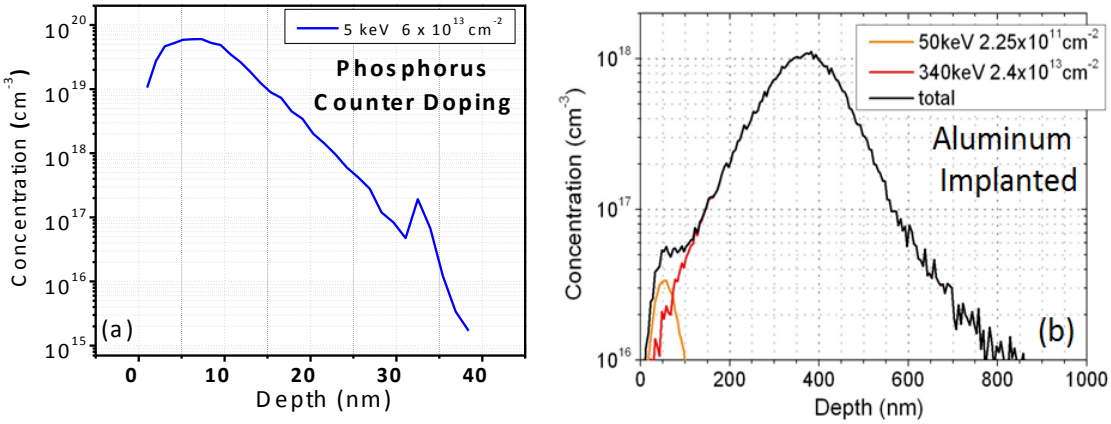


Fig 5.10. Doping profile of MOSFETs fabricated with Phosphorus surface counter doping (a) or with and aluminum implanted p-well (b).

5.2.4. MOS capacitor electrical characterization

In a first phase we have characterised the MOS capacitor test structures. The C(V) of the 3 different sets is plotted in [Fig.5.11.a]. In all the cases, the flatband voltage shifts toward negative values, accounting either for negative mobile charges that reach the SiO_2/SiC interface

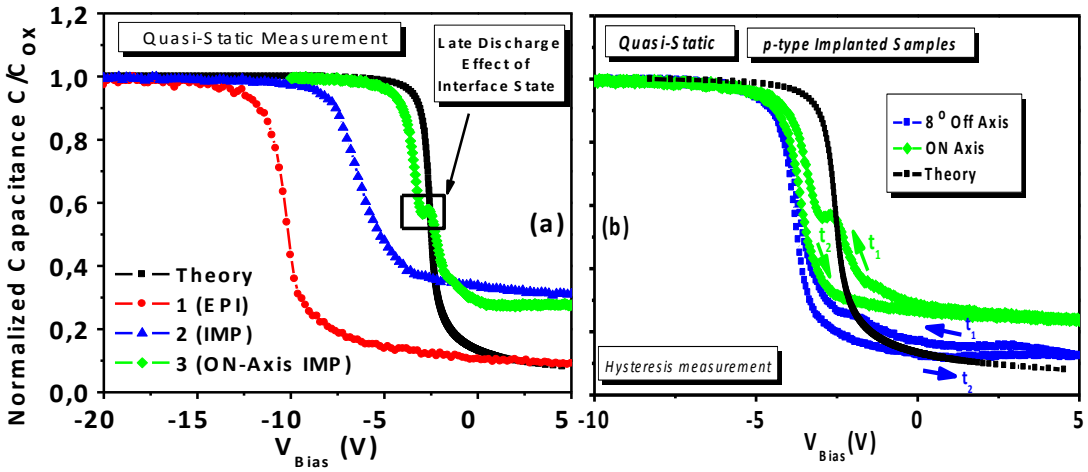


Fig.5.11. Normalized C-V characteristics showing the evidence of late interface discharge on on-axis samples.

during the negative bias stress or for electron detrapping at the SiO_2/SiC interface. The flatband voltage (V_{FB}) of the on-axis MOS capacitor is the closest one to the theoretical values and has a relative low variation during the C(V) hysteresis cycle [Table 5.1]. The other samples show higher V_{FB} shift, giving an indication about a higher amount of effective oxide charges in the dielectric layer since the oxide thickness is approximately similar for all the samples. Indeed, the epilayer MOSFETs with phosphorus counter doping show a large V_{FB} shift in comparison with the theoretical V_{FB}. This confirms that Phosphorus inclusion, either by $POCL_3$ annealing process or by implanted Phosphorus surface counter doping strongly acts on the V_{FB} shift. However, the flatband voltage hysteresis (ΔV_{FB}) observed is much lower in this phosphorus implanted case than in the $POCl_3$ case of P2 process (section 5.1.3), with an amount of N_{eff} 7 times lower. The on-axis sample has shown excellent electrical characteristics from the charge traps perspective. A very small hysteresis has been observed together with a very low amount of N_{eff} and N_{fc} that are respectively 4 and 13 times lower than in the 8ºOff axis EPI case, and 3 and 8.5 times lower than in the 8ºOff IMP case (sample 2). If we compare the obtained N_{eff} for the different processed samples, the one corresponding to the on-axis sample is much lower, indicating that during the oxidation process fixed and trap oxide charges are less susceptible to interfere in an on-axis sample. The values of the other samples are in the same range than the ones founded in the literature [28]. However, on the C(V) characteristics presented in [Fig 5.11.a and b], the on-axis sample presents a small bump in the depletion zone, whereas the

Sample	Type (Axis)	V_{FB}	ΔV_{FB}	$V_{\_Oxide\_Br}$	T_{ox}	N_{eff}	N_{fc}
1	Epi (8° Off)	-10.6	-0.9	28.3	42.5	1.2	5.5
2	IMP (8° Off)	-6.8	-0.3	29.2	42.4	0.9	3.4
3	IMP (On)	-3.1	-0.2	30.4	43.7	0.3	0.4
Unit		V	V	V	nm	$\times 10^{12}.cm^{-2}$	$\times 10^{-9}.cm^{-2}$

Table 5.2. Electrical parameters extracted from the C(V) electrical characterization.

others samples does not. This is a consequence of the late discharge of the deep interface states located within the bandgap [29-30]. C(V) fluctuations can also been observed. Indeed, if we consider a surface Al p-type doped, a very high quantity of holes is in direct contact with the SiO_xN_y transition layer. All of them are able to tunnel into the SiO_2 layer. As S.Berberich explained in his work [29], within a narrow range of surface potential, most of the negatively charges surface states can be discharged by hole capture. This hole capture associated with the arrival of new hole inside the Al-implanted layer due to the gate negative bias provokes, at a given surface potential, a fluctuation of the capacitance whose amplitude depend on the amount of tunnelled positive charges to the SiO_2 layer. Concerning the observed bump in the on-axis sample, it is worth to explain why the bump does not occur in the other samples. We assumed this event to be due to a higher deep level defect density at the SiO_2/SiC interface in the on-axis sample. According to the results obtained, we suggest the existence of a higher deep level defect density at the SiO_2/SiC interface in the on-axis sample than in the 8º Off axis probably due to the dislocation defects necessary to grow an on-axis sample. Therefore, according to the energy band diagram for SiC MOS device in the depletion zone [31], there may have higher charge/discharge effect of the negatives interface traps in the on-axis sample.

The last comment regarding the C(V) curves concerns the oxide thickness. Indeed, it seems that the oxide grows a little bit faster on on-axis sample. However, the oxide thickness difference can be explained in terms that the wafers were not processed at the same time inside the oxide furnace. The RTP furnace temperature ramp is regulated by a PID controller, and it does not have exactly the same reaction time. Depending on it, the gate oxidation could have been performed faster or slower, resulting in a very small variation of the oxide thickness.

5.2.5 MOSFETs room temperature measurements and stress

The electrical characterization has been carried out on lateral MOSFET having a gate width of 150 µm and gate length varying from 2 µm to 24 µm. Typical transfer curves $I_{DS}(V_{GS})$ and forward curve $I_{DS}(V_{DS})$ at V_{GS} = 8 V of a 24 µm channel MOSFET are presented in [Fig 5.12] for the 3 types of configurations. From these curves we have extracted threshold voltage, effective channel mobility and oxide breakdown capability of the MOSFETs. In comparison with the 8ºOff Axis Al-implanted MOSFETs, the on-axis Al implanted MOSFETs' maximum saturation I_{DS} is more than 14 times higher. The only parameter that can explain such a difference is the surface roughness improvement leading to higher μ_{fe}.

Wafer uniformity

Due to the starting material defects density (especially in the case of on-axis MOSFETs) plus the processes non uniformities, we observed a large dispersion in the electrical results along the wafer area. Indeed, the on-axis MOSFETs electrical characterization allows to evidence the crucial problem of the epi-grow uniformity. Acceptable results ($0V > V_{TH} > 4V$ with $8\ cm^2.V^{-1}.s^{-1} > \mu_{fe} > 18\ cm^2.V^{-1}.s^{-1}$ at V_{GS} in the range of [15V; 25V]) could have been obtained

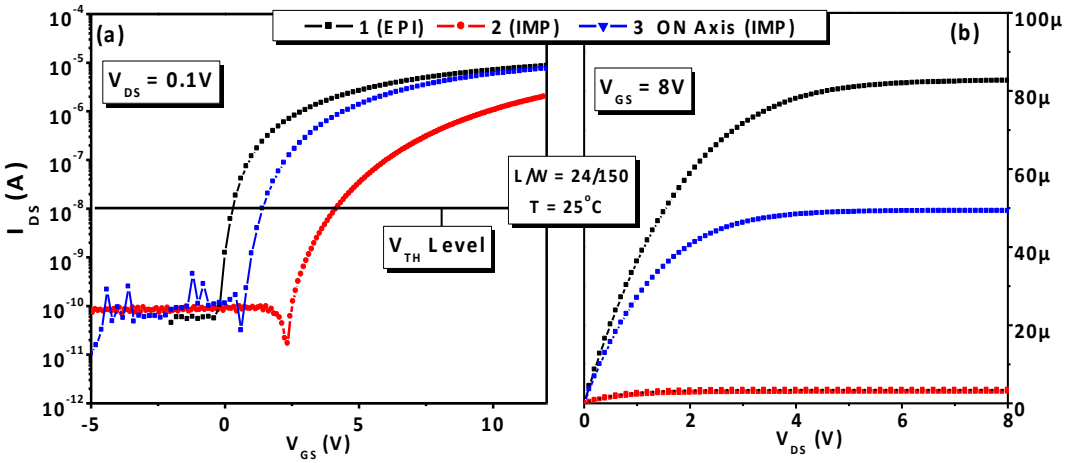


Fig. 5.12: I_{DS} (V_{GS}) (a) and I_{DS} (V_{DS}) (b) characteristics of the 8° Off axis epilayer MOSFETs, 8°Off axis implanted MOSFET and on-axis MOSFETs.

only on 25% of the processed wafers. The other 75% cannot be considered as acceptable because V_{TH} > 25V and the peak μ_{fe} < 0.1 $cm^2.V^{-1}.s^{-1}$. In order to give an idea about the wafer uniformity, Gaussian distribution of the epitaxied and implanted MOSFETs electrical parameters have been plotted in [Fig 5.13]. The uniformity analysis test have been performed on MOSFETs having L = 24 µm and W = 150µm. In the case of on-axis MOSFETs, the Gaussian distributions have been plotted only by taking into consideration the 25% of the normal operating MOSFETs.

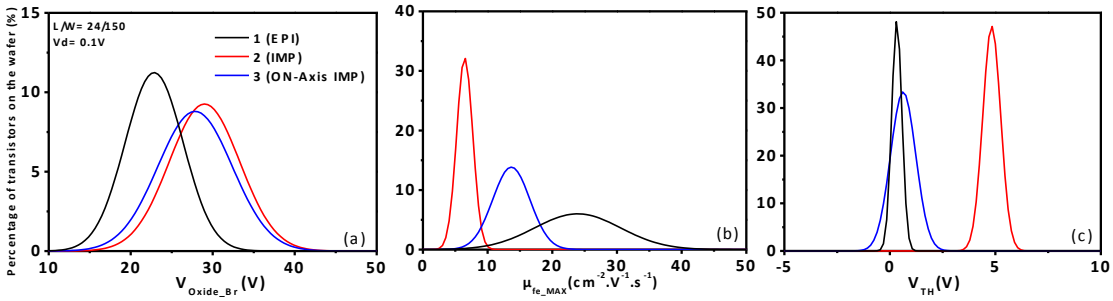


Fig 5.13: *Gaussian distribution of V_{oxide_Br} (a), μ_{fe} (b) and V_{TH} (c) for uniformity evaluation of all the measured MOSFETs.*

Threshold voltage

The V_{TH} values of the MOSFETs samples have shown quite good uniformity [Fig 5.13.c]. Few EPI and on-axis MOSFETs showed slightly negative V_{TH}. Nevertheless, most of the MOSFETs have shown positive V_{TH} for all channel lengths (2 µm- 24 µm). Most of the V_{TH} values observed in the case of the EPI MOSFET analysis are very close to 0. In comparison with the epilayer sample processed **without** phosphorus counter doping, the V_{TH} is lowered by 1.5V. This result confirms the assumption that phosphorus surface counters doping act as a donor at the SiO_2/SiC interface, and tends to shift the V_{TH} toward the negative values.

Oxide breakdown analysis

As it can be seen in Fig 5.13.a, the sample with surface counter doping exhibits a lower oxide breakdown capability. Phosphorus implantation process might have created either interface state charges with a donor tendency (large negative flatband voltage shift) at the SiO_2/SiC interface that contributed to lower the oxide barrier and decrease the V_{oxide_br}, or ion mobile charges that might have tunnelled from the P-surface to the oxide volume during the post oxidation annealing and decreased the oxide barrier. Although Aluminium has been implanted in the others samples 2 and 3, the V_{oxide_Br} didn't change in comparison with the samples tested on P-epilayer in section 5.1.4.

Channel peak mobility

In this specific experiment, the highest peak mobility is obtained on the epitaxied surface with Phosphorus counter doping. In the current literature, most of MOS interface improvement experiments are carried-out on epitaxied substrates, and there are few results of μ_{fe} extraction on Al implanted MOSFETs. What is more common are μ_{fe} values obtained from vertical power MOSFETs [32] having an implanted P-well. Nowadays, the maximum μ_{fe} of such Al implanted MOSFETs is in the range of [1 $cm^2.V^{-1}.s^{-1}$; 5 $cm^2.V^{-1}.s^{-1}$] [32-33], so typically much lower than experiments done on epitaxied N-MOSFET samples. These mobility degradations on implanted P-layer are confirmed by our μ_{fe} results of sample 2 (IMP 8ºoff), being in the range of [6 $cm^2.V^{-1}.s^{-1}$; 9 $cm^2.V^{-1}.s^{-1}$]. However, in the case of the (Al implanted) on-axis MOSFETs, the mobility range of [9 $cm^2.V^{-1}.s^{-1}$; 19 $cm^2.V^{-1}.s^{-1}$] is higher, and may be due to the better surface roughness. So far, this is the first time that such a high μ_{fe} on the implanted MOSFETs is reached at CNM. On the other hand, if we compare the μ_{fe} room temperature results of the 8ºOff axis MOSFETs having Phosphorus surface counter doping [Fig 5.14.a.] to the one that do not contain phosphorus [Fig 5.6.b], we see that the μ_{fe} at high field (V_{GS} > 12V) is generally slightly lower after the phosphorus doping, although it presents in the best case a higher peak μ_{fe}.

Interface charges

D_{it} distributions have been extracted using the subthreshold technique described in section 2.4.2, and are compared in [Fig 5.14.b]. The qualitative values are in accordance with the μ_{fe} ones, as when D_{it} is lower, μ_{fe} is higher. MOSFETs having Phosphorus surface counter doping show lower D_{it} values in comparison with that of the non-implanted phosphorus (P3) [Fig 5.4.b]. As D.Okamoto reported in his work [6], this D_{it} improvement may be due to the incorporated P atoms which probably reduce a strain existing in SiO_2 near the interface [34]. For the implanted MOSFETs (2) which show relatively low μ_{fe}, the D_{it} obtained is higher than that of MOSFETs from samples (1) and (3). Measured MOSFETs from sample (3), although implanted, exhibit low D_{it} values, around 2×10^{11} $eV^{-1}.cm^{-2}$. However, a lot of progress still needs to be performed on implanted samples in order to get its D_{it} values as low as in epilayer samples. The higher D_{it} observed in the case of the Al-implanted MOSFETs (higher in the off-axis sample than in the on-axis one) is typically explained by the fact that the implantation process obviously provokes much more damages in the crystal lattice than the one generated by the

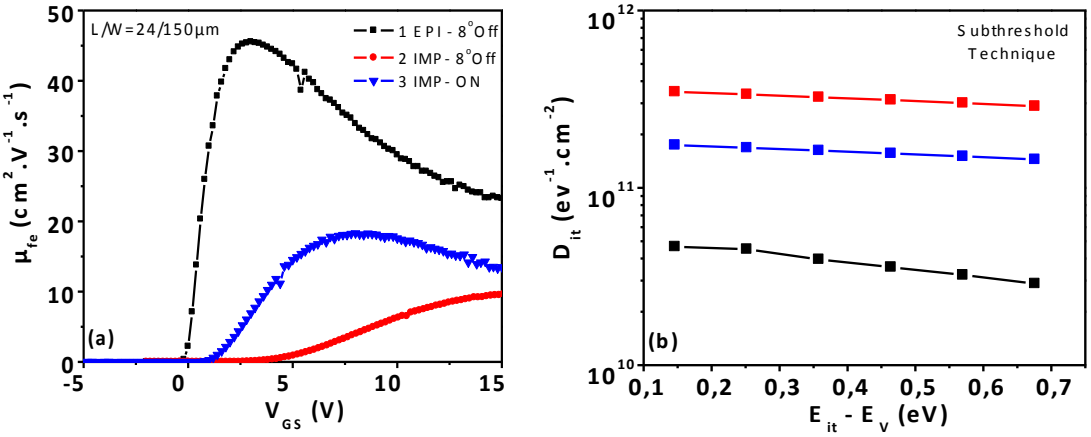


Fig 5.14. The field effect mobility variation in function of the gate source voltage (a) and the D_{it} variation above the valence band obtained by the subthreshold technique (b)

epi-growth process. We also assume that the μ_{fe} difference between 8° off-axis and on-axis implanted samples is due to the higher surface flatness of the on-axis sample, thus reducing the roughness scattering mechanism. In the literature on nMOSFETs with implanted p-well, no report mentioning a μ_{fe} variation superior to our presented above has been found. This is mainly because all the presented μ_{fe} are extracted from the transconductance curves of epitaxied MOSFETs (ideal case). The combination of the Nitrogen high passivation properties together with the on-axis surface finishing (assuming that the MOSFET is located in an area of the wafer where a few amount of defects are created during the on-axis epi-growth), gives our on-axis MOSFET a high potential for high performances MOS gated devices.

Stability tests

Once the static characterization performed, we proceed to the BSI electrical measurement in order to monitor the V_{TH} stability as well as the GIDL currents. In general, bias-stress instability also alters the drain leakage condition mechanism and results in an enhancement of the GIDL current as reported in [35]. We assume that this effect is due to the cumulative negative charge at the SiO_2/SiC interface during the positive stress bias and to the interface traps.

Thus, a first encouraging result is the absence of GIDL in the Al implanted on 8° Off axis substrate. However, in the case of the epitaxied MOSFETs with phosphorus surface counter doping (1) [Fig 5.15.a], the GIDL even increased in comparison with the epi-MOSFETs without counter doping [Fig 5.5.b], raising a drawback of the phosphorus implantation counter doping. However, the GIDL obtained is still acceptable because its value after the longest PBSI time remains below 10 nA [Fig 5.15.a]. This GIDL values appeared to be lower in the case of the on-axis MOSFETs (3) [Fig 5.15.c], but still higher than in the case of MOSFETs IMP (8° off-axis) [Fig 5.15.b]. The deep cause of the GIDL generation is not known but could be connected to the oxidation process, surface roughness and to charge trapping during BSI stress.

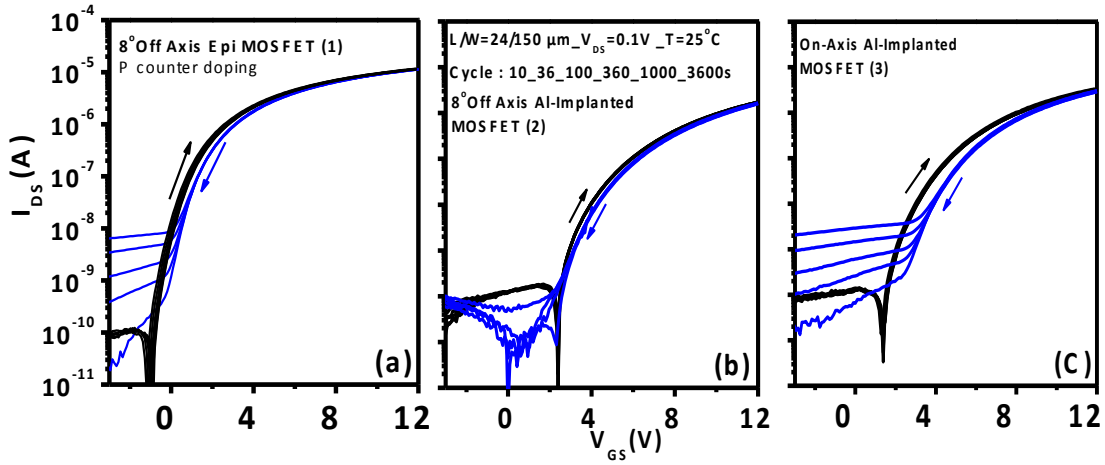


Fig 5.15. Transconductance characteristics after BSI stress of epilayer MOSFETs (a), Al implanted MOSFETs (b) and on-Axis Al implanted MOSFETs (c).

The V_{TH} extracted before and after the BSI experiment exhibit small hysteresis variation. The time evolution of these electrical parameters is represented in [Fig 16]. In term of time stability, all the samples have shown similar variation of V_{TH_NBSI} [5.16.a]. However, the time dependent variation of ΔV_{TH} appeared to be more stable for the on-axis MOSFETs (3) than the other stressed MOSFET. More specifically, the ΔV_{TH} stability of (3) seems to be almost constant within the time stress in the range of [100s; 3600s], whereas the other MOSFET (1) and (2) have shown more visible ΔV_{TH} variations [5.16.b]. Indeed, after a certain stress time, the hysteresis amplitude of MOSFET (3) seems also to remain similar, whereas for the other samples, there is a clear variation of the hysteresis through time. Thus, it is clear that the on-axis MOSFET (3) is the one whose amount of $|N_{it}+N_{ox}|$ generated by the BSI stress is the lowest among the tested MOSFETs. The total amount of $|N_{it} + N_{ox}|$ generated during the stress can be deduced from ΔX (with $X \in \{1,2,3\}$) representing the ΔV_{TH} difference drift with time (for example $|\Delta 1| = |\Delta V_{TH}$ at t =10s – ΔV_{TH} at t=3600s|).

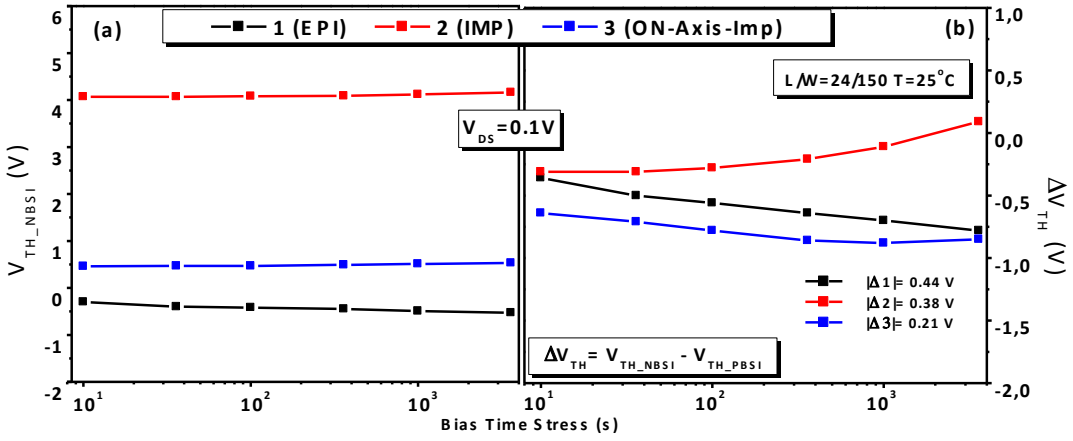


Fig 5.16. Threshold voltage variation after a negative bias stress (a) and the threshold voltage hysteresis variation with time (b) of the epilayer MOSFETs, Al implanted MOSFETs and on-Axis Al implanted MOSFETs (c).

5.2.6. Temperature dependence measurements

The variation of the μ_{fe} at high temperature helped us to observe extra properties of the processed samples [Fig 5.17.a], specifically regarding the surface roughness. The high temperature and BTI experiments have been performed on different MOSFET device than the one used for the BSI experiment. Their geometrical parameters are L=12μm and W=150μm.

Threshold voltage

For the phosphorus surface counter doped MOSFETs (1), the V_{TH} dependence with temperature is curious because, following the physics rule (see section 2.5) it decreases when the temperature increases up to T=150ºC. But at high temperature V_{TH} tends to increase with the temperature increase in the range of 150ºC up to 250ºC. This behavior is unexpected since the interface states are supposed to be filled with the increase of temperature. This interface charge filling effect might continuously decrease the V_{TH} over the temperature rise, as we can observe in the case of the Al implanted samples (2) and (3) [Fig 5.17.b]. Therefore, the V_{TH} instability observed in the case of counter doped MOSFETs (1) can only be connected either to the epilayer or to the phosphorus surface doping effect. We suggested that the implantation of phosphorus, together with the N_2O oxidation could create complexes at the SiO_2/SiC interface corresponding to very deep interface level that might be activated only over 150ºC. This behavior was also reported in chapter 3 (see section 3.4.6). Still, deep level transient spectroscopy (DLTS) analysis is required in order to confirm this hypothesis. A second suggestion is that epilayer defects such as screw dislocations or edge dislocations might also disturb the crystalline lattice and be enhanced by the phosphorus implantation process. These defects might bring additional deep level that, with the high temperature, could activate and impact the SiO_2/SiC interface. From the V_{TH} point of view, the on-axis Al implanted MOSFET (3) seemed to present the best V_{TH} stability with temperature. Indeed, in comparison with the 8ºOff axis, Al implanted MOSFET (2) and MOSFETs (3) shown a lower V_{TH} at low temperature and a much smaller decreasing rate with the temperature increase. The V_{TH} difference between

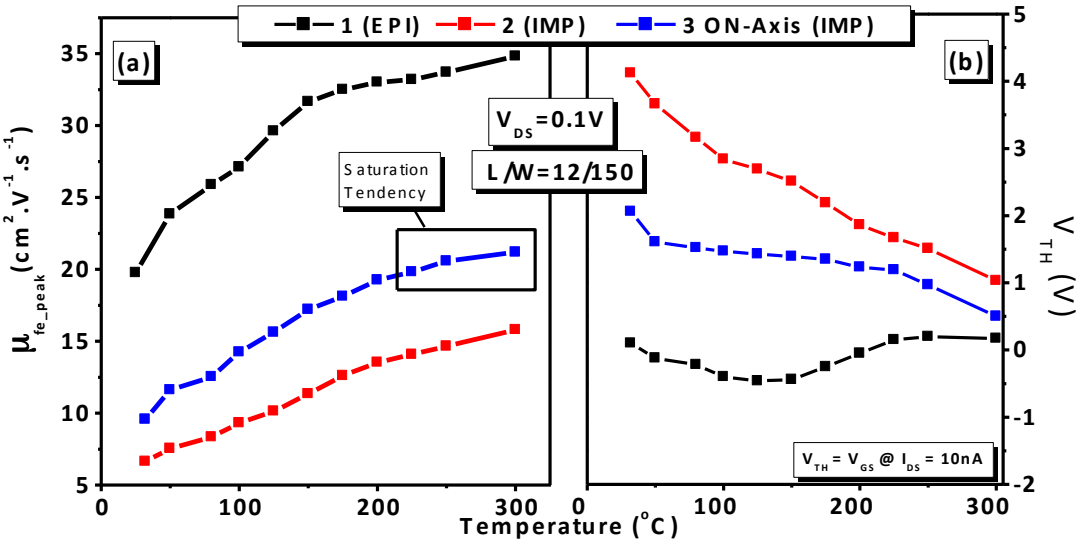


Fig 5.17. Peak field effect mobility (a) and threshold voltage variation (b) as a function of the temperature.

the room temperature value and the one at 300ºC is equal to 1.5V in the case of MOSFET (3) whereas for MOSFET (2), this difference is above 3V. Moreover, contrary to MOSFET (1), MOSFET (3) remained normally-off at any temperature below 300ºC.

Channel peak mobility

In a general case of SiC nMOSFET, an increase of μ_{fe} is typically observed while raising the temperature. As already mentioned in section 2.5, *Matocha et al* explained in [36], that the dramatic μ_{fe} decrease at high fields is due to the predominance of surface roughness scattering, through its strong electric field dependence ($\mu_{SR} \sim 1/E^2$) [37]. This dominance of surface-roughness scattering is amplified due to the high surface fields required to invert the SiC surface (2 times higher than that of Si). Hence, a drastic decrease at high temperature and high field of the μ_{fe} for all our samples is observed. In [Fig 5.18], we plotted the μ_{fe} variation with time at 200ºC [Fig 5.18.a] and 300ºC [Fig 5.18.b]. At high electric field, and high temperature, the surface roughness-scattering effect is so strong that even MOSFET (3), with its flatter SiO_2/SiC interface, has a μ_{fe} similar (higher by 1.03%) than the other 8°Off Axis MOSFETs (1) and (2) in the gate voltage range of [15V ; 20V]. At this temperature, the type of MOSFET (epilayer or implanted layer) does not seem to matter since they all tend to the same value (around 10 $cm^2.V^{-1}.s^{-1}$). More surprisingly, this value is lower than the one obtained on the 8ºOff axis MOSFET without P surface counter doping.

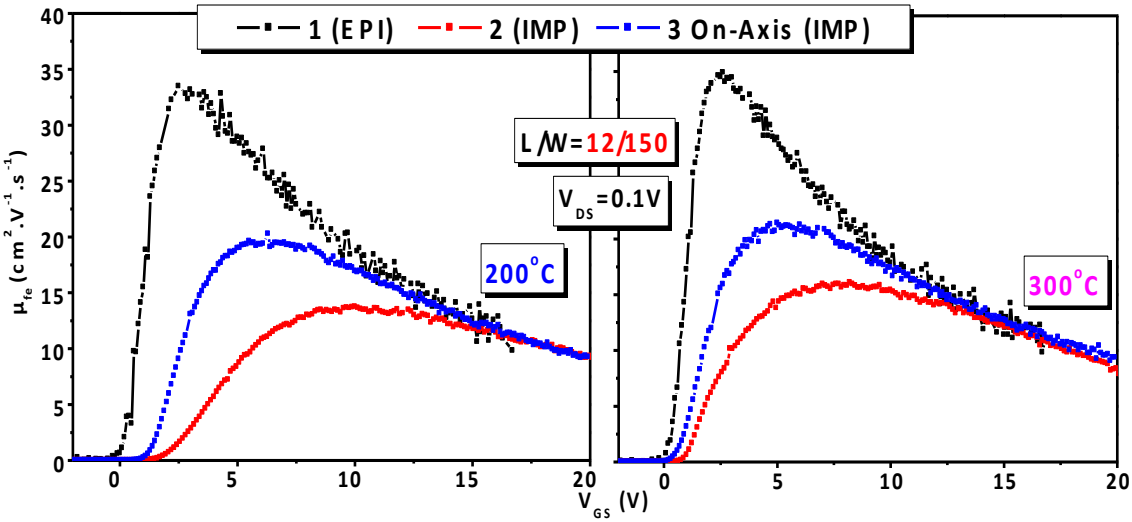


Fig 5.18. Field effect mobility variations in function of the gate voltage for the 8ºOff Axis epilayer MOSFET (1) with phosphorus counter doping, the 8º off-Axis Al-implanted MOSFET (2) and the on-axis Al-Implanted MOSFETs (3) at 200ºC (a) and 300ºC (b).

Ohmic contacts

In order to discard any parasitic effect of the processing and especially ohmic contact formation on the results we observed, a TLM analysis has been performed (see section 2.2). As the metallization process is supposed to be the same for all the fabricated MOSFETs, the TLM characteristics evolution with temperature should be identical for all samples. Then, the TLM I-V

characteristics have been measured at all temperature. Absolutely no rectifying effect has been observed at any temperature for any sample. In [Table 5.3], we summarized the different contact resistivity values extracted for all samples at different temperatures. The observed difference between MOSFET (1) and the others is that the phosphorus surface counter doping (n-type doping) might have contributed to reduce the contact resistivity and thus decreased the contact resistance. However, in this case, it seems that the contact resistivity increased with temperature up to 50ºC before stabilizing, whereas in the case of MOSFETs (2) and (3), the contact resistivity, tended to decrease with the temperature increase, typically observed. Nevertheless, the anomalous V_{TH} variation of counter doped MOSFETs with temperature cannot be explained by the ohmic contact behavior as no rectifying effect is observed.

ρ_c ($\Omega.cm^{-2}$)	Temperature				
Sample	25ºC	50ºC	100ºC	200ºC	300ºC
1	0.12×10^{-4}	0.54×10^{-4}	0.56×10^{-4}	0.58×10^{-4}	0.59×10^{-4}
2	1.48×10^{-4}	1.42×10^{-4}	1.37×10^{-4}	1.20×10^{-4}	1.18×10^{-4}
3	1.49×10^{-4}	1.44×10^{-4}	1.39×10^{-4}	1.25×10^{-4}	1.21×10^{-4}

Table 5.3. Summarized table of the temperature impact on the contact resistivity values.

5.2.7. Time bias stress at high temperature

The combination of time BSI and BTI measurement has been carried out on other MOSFETs located at the vicinity of the previous ones, explaining the differences in term of threshold voltage. The temperature chosen for this type of stress was 200ºC in order to be sure not damaging the oxide during the BSI stress. The V_{GS} measurement range is [-5V ; +15V]. As the component is not packaged, the main difficulty is to guarantee a good contact between the tip probe and the MOSFET. Indeed, due to the high temperature, the tip probe may move during the BSI stress. For this reason, it is compulsory to monitor and insure the tip contact over the gate, drain, source and bulk PAD every 5-10 minutes during the measurement.

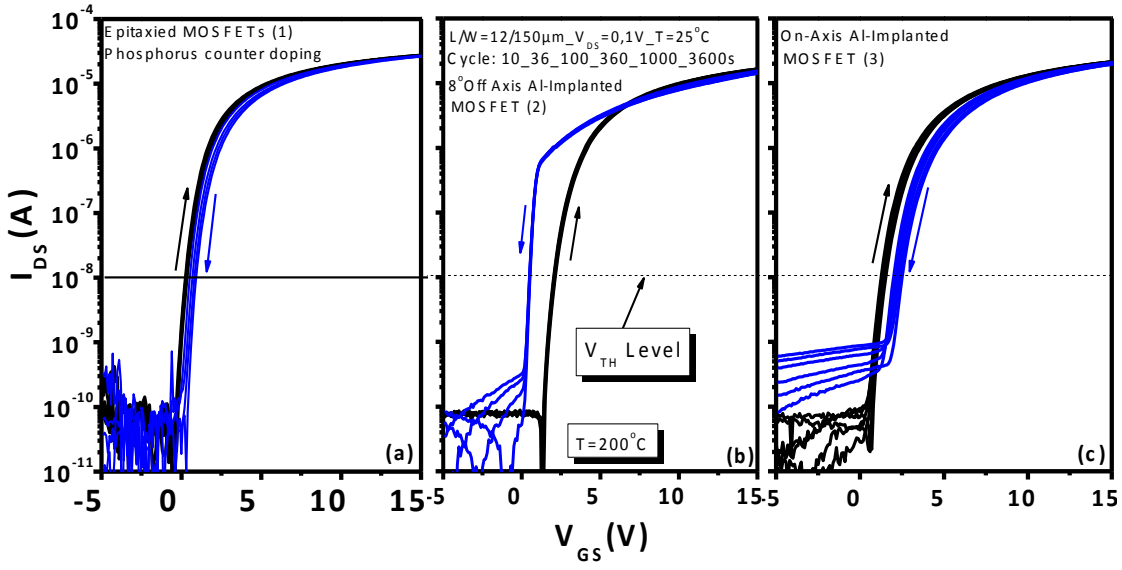


Fig 5.19. Transconductance characteristics after high temperature BSI stress of epilayer MOSFETs (a), Al implanted MOSFETs (b) and on-axis Al implanted MOSFETs (c).

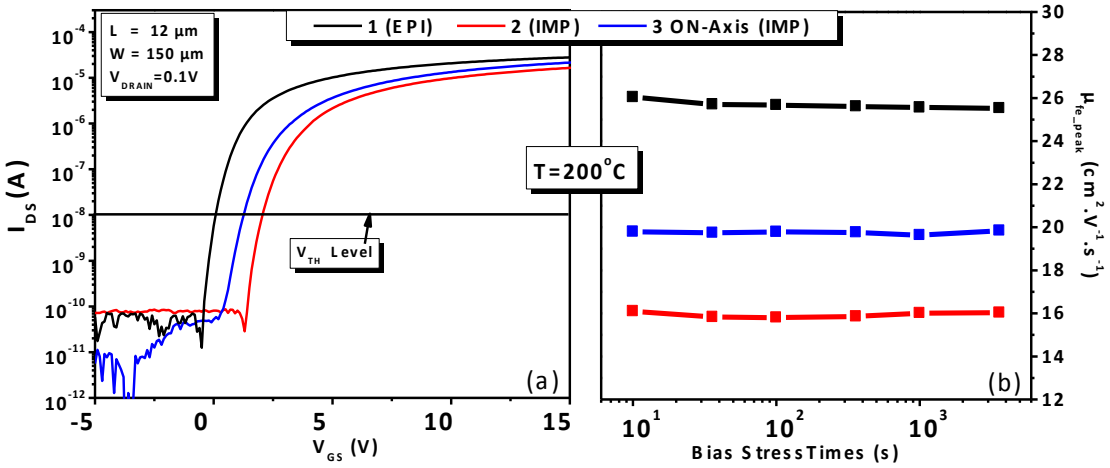


Fig 5.20. μ_{fe_peak} (t) time stability with BSI stress (b) of the 8º Off axis epilayer MOSFETs, 8ºOff axis implanted MOSFET and on-axis MOSFETs at 200ºC.

The I_{DS} (V_{GS}) electrical characteristics are depicted in [Fig 5.19]. It can be observed that, in the case of 8º Off axis Al-implanted MOSFET (2), the I_{DS} (V_{GS}) drift is opposite to that of MOSFETs (1) and (3): A negative shift curves is observed after a NBS in the case of MOSFET (2) indicating that negative charges and near interface charges predominate and interfere during the positive bias stress. Meanwhile, a positive shift of the I_{DS}(V_{GS}) is observed for the other type of MOSFETs, with a lower drift of MOSFET (3) (on-axis). As the difference between MOSFET(2) and MOSFETs (3) is only the cut axis of the epi-substrate, we suggest that the charge type interfering at the SiO_2/SiC interface during high temperature time BSI might be dependent the surface roughness of the Al-implanted MOSFETs.

At 200°C the GIDL current is not relevant, because the interface charges scattering is not a predominant effect at high temperature. The extracted I_{DS} (V_{GS}) curves from the first ramp up of the BSI stress at 200ºC of the different MOSFETs (1), (2) and (3) have been gathered and plotted in a single graph [Fig 5.20.a]. On this graph, the transconductance difference between the MOSFETs types is evidenced. In comparison with the same measurement at 25ºC [Fig 5.13], this transconductance difference is smaller at 200ºC. On the other hand, at this temperature, the peak of field effect mobility (μ_{fe_peak}) appeared to be very stable with time and do not change with the increase of time stress. Another observation concerns V_{TH_NBSI} and ΔV_{TH}, which appear to be quite stable, with no gate leakage and with a very small variation with stress time [Fig 5.21]. Still, despite of the high stability of all the samples, MOSFET (2) and (3) appear to be the most stable ones, with a low hysteresis variation of about 0.2V (versus 0.3V for (1), which is acceptable). A good ΔV_{TH} stability is also observed, even in the case of the Phosphorus surface counter doped MOSFETs (1). Its amplitude values remain almost equal than the measured one at 25ºC. The same positive comment can be done for the Aluminum implanted on-Axis MOSFETs (3). However, despite of the ΔV_{TH} time stability improvement observed, the ΔV_{TH} amplitude have been increased by more than 1.5V in comparison with the measure performed at 25ºC.

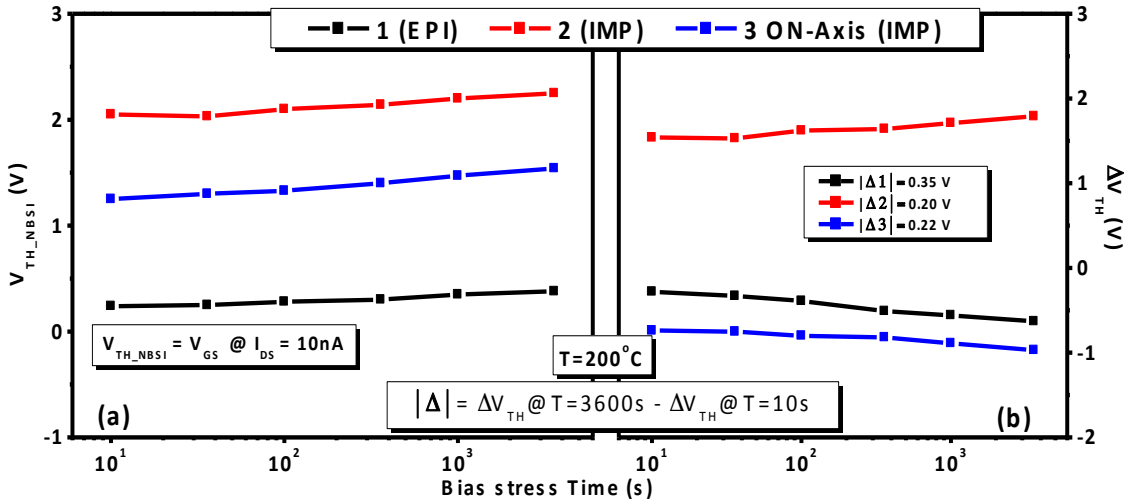


Fig 5.21. V_{TH_NBSI} (a) and ΔV_{TH} (b) time stability variation of the 8º Off axis epilayer MOSFETs, 8ºOff axis implanted MOSFET and on-axis MOSFETs at 200ºC.

Finally, After the BSI stress at 200ºC, the chuck temperature was cool down to 25ºC and, BSI has been performed again at 25ºC on the same component. Results had shown a ΔV_{TH} variation identical to that of 1st measurements presented in [Fig 5.16], for all MOSFET, showing reproducibility of ΔV_{TH} values and drift. Moreover, in the case of the implanted on-Axis MOSFETs (3), the temperature didn't seem to negatively impact the ΔV_{TH} time stability.

5.3. Conclusions

Our state of the art gate oxidation process used in previous works could have been optimized by performing a longer Argon annealing (10 min instead of 3 min). This new gate oxide demonstrated higher μ_{fe}, lower D_{it} values, similar Time Bias V_{TH} stability but lower V_{TH} variation under BTI stress in comparison with the previous processes. Once the new gate oxide has been designed, several MOSFETs processing experiment based on Al implantation, surface counter doping with Phosphorus and modification of cut axis of n-epi substrate have been carried out in order to see if further optimization was possible. The properties and drawback of implanted structure with on-axis n-substrate have been studied. Especially, the best MOSFETs have presented a peak of μ_{fe} at 19 $cm^2.V^{-1}.s^{-1}$, which is pretty high for implanted MOSFETs technology. In all the presented MOSFETs, the V_{TH} stabilities of are much better than the one observed in the previous chapter regarding the case of the non-irradiated MOSFETs. In addition, the phosphorus surface counter doping helped to increase the peak channel mobility μ_{fe}. However, the main drawback of the entire process is that the uniformity of the process do not guarantee to obtain such a high μ_{fe} value everywhere on the wafer of MOSFETs due to the difficulties of growing an n-substrate (creation of screw or edge dislocations during growth).

These analyzed samples seemed generally to show better characteristic than any of the presented MOSFETs in the previous chapter. Furthermore, very encouraging results shown

how stable at high temperature can be the new designed gate oxide. Moreover, although the P counter doping have shown small instabilities issues at 25ºC, it seems that these instabilities do not appear under high temperature operation.

Taking into account these promising results, it has been decided to perform several irradiation and annealing processes on these MOSFETs. Results are exposed in the next chapter, It is suggested that maybe, and even if the irradiation impact might not be so relevant due to the good MOSFETs quality, the results could help us to understand better what have been observed in the previous experiments (chapter 3 and 4).

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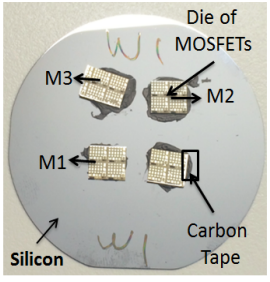
CHAPTER 6
Irradiation of 4H-SiC MOSFETs with optimized gate oxide: Limit of Robustness

Proton irradiation and post irradiation annealing impact on the new generation of MOSFETs studied in the previous chapter is evaluated. The analysis performed on the new devices confirms the existence of a threshold fluence that might changes the type of SiO_2/SiC interface charge from donor to acceptors at any irradiation energy. Moreover, the irradiation process has shown one additional property: It induces GIDL lowering during the time bias stress experiment and this GIDL did not increase after the post oxidation annealing. Finally the conclusion about irradiated MOSFET with oxynitrided gate oxide will be given.

6.1. Irradiation Set-Up of SiC MOSFETs with the new gate oxide process

This time, the irradiation experiment is slightly different, with only 2 irradiation energies performed on the presented new MOSFETs in the previous chapter. Once completed the fabrication process and performed the first devices electrical characterization, the samples were diced into dies, pasted on Si wafer with carbon tape, and sent for the irradiation experiments. We have shown one picture of Si wafer, just below in [Fig 6.1]. In this picture, there are four dies but only 3 of them have been studied in the frame of this thesis: Their specificities are described next to the picture. The non-analyzed one is an aluminum implanted MOSFETs with a similar Al implantation profile and gate oxide process as the MOSFETs (2). However, the gate metal of this MOSFET was made with tungsten (MOSFETs-W). For the sake of clarity, and in order to no complicate too much the comparison and try to establish clear hypothesis and conclusions, the MOSFET with a tungsten gate metal have not been studied in this thesis. The W1 mark on the Si wafer is just a name corresponding to a specific irradiation process (energy and fluence). The irradiation processes performed are indexed in table 6.1.



M1 = MOSFETs (1) : 8ºOff Axis Epilayer plus Phosphorus counter doping

M2 = MOSFETs (2) : 8ºOff Axis Implanted Layer with Aluminum Doping

M3 = MOSFETs (3) : On-Axis Implanted Layer with Aluminum Doping

Fig 6.1. Picture of on wafer (among others) that has been submitted to the irradiation and post irradiation annealing process, with a short description of the MOSFETs characteristics.

Particle type	Proton	
Energy (MeV)	0.18	10
Fluence (cm^{-2})	Mrad	Mrad
5×10^{12}	36.81	5.14
5×10^{13}	368.1	51.45
5×10^{14}	3680.2	514.50
5×10^{15}	36802.3	Not irradiated

Table 6.1. Summary of the proton irradiation parameters: Energy, Fluence and conversion to radian following the formula given in section 3.2.1.

The main difficulty was to select MOSFETs on the different samples having more or less the same electrical behavior in order to perform BSI and BTI analysis before and after the irradiation process. As it was shown in the previous chapter, the wafer uniformity was one of the main issue, especially in the case of the on-axis MOSFET (3), where only 25% of the MOSFETs have shown reliable electrical characteristics (against 80% for MOSFET (1) and MOSFET (2)). The poor uniformity of the on-axis wafer led to a reduced number of irradiation process. Overall, a total of 1152 MOSFETs, including 72 MOSFETs having similar geometrical parameter and electrical characteristics, have been irradiated, excluding MOSFETs-W. Then, 10 Si wafers containing 3 individual dies were irradiated with protons at various energies and fluences (see Table 6.1). This number was large enough to extract additional information and confirm some observed behavior after the irradiation and after post irradiation annealing (PIA). From the threshold voltage and field effect mobility point of view, the conclusions in most of irradiation cases are the same than those obtained in chapter 3 and 4 on both gate oxides in the proton irradiation range of [$5 \cdot 10^{12}$ cm^{-2} - $5 \cdot 10^{14}$ cm^{-2}].

Before irradiation, BSI and BTI measurements have been performed on all the MOSFETs. After irradiation, the SiC-MOSFETs were electrically characterized and post-annealed under N_2 at 120ºC firstly for 14 h and subsequently for 90 h. The MOSFETs were measured before irradiation, after irradiation and after each annealing step, using the BSI technique, and following the time cycle defined in section 2.6. After the final annealing and the last BSI measurement, they were measured under BTI, from 25ºC to 250ºC (see chapter 3 and 4), extracting the same electrical parameters as previously. The next sections describe the MOSFETs behavior before irradiation, after irradiation and after annealing. Due to the huge amount of data, an annex has been included at the end of the chapter. For the sake of clarity, this annex follows this approach:

1 → C (V) analysis after irradiation to monitor the irradiation impact on the flatband voltage shift. In most of the cases, it was very difficult to obtain reasonable C(V) curves: Thus, only few C(V) characteristics are presented.

2 → I_{DS} (V_{GS}) curves after each irradiation fluence together with the gate leakage current and field effect mobility.

3 → D_{it} values above the valence band edge. This parameter is not always calculated due to the small amount of proper C(V) characteristics obtained.

4 → I_{DS} (V_{DS}) curves in order to prove that even the irradiated MOSFET kept on having a transistor-like behavior.

5 → The I_{DS} (V_{GS}) curves under BSI off irradiated and non-irradiated MOSFETs are presented: V_{TH_NBSI} and ΔV_{TH}.

6 → C(V) behavior of the post-irradiation annealed MOSFETs is shown when possible.

7 → μ_{fe} (V_{GS}), V_{TH_NBSI} (t) and ΔV_{TH} (t) of the NI MOSFETs, irradiated MOSFETs and post irradiation annealed MOSFETs are presented.

8 → The μ_{fe} (V_{GS}) evolution at different temperature for each irradiated MOSFET is shown at different fluence and energies.

9→ The threshold voltage variation V_{TH} with temperature is presented for several absorbed fluences.

Although a huge amount of data is reported in the annex, only the most relevant ones will be detailed. Most of the I_{DS} (V_{GS}) measurements have been performed in the range of [-10V ; +15V] with V_{DS} = 0.1V, with a gate source compliance equal to 1µA.

6.2. Epitaxied MOSFETs with oxynitrided gate oxide and phosphorus surface counter doping

The MOSFET EPs presented below accounts for devices with a gate length (L) and width (W) of L/W = 24 µm /150 µm. It is reminded that MOSFETs having a phosphorus surface counter doping are called “MOSFET (1)”. In all the cases, the V_{TH} has been defined as the gate voltage at which I_{DS}=10nA (V_{DS}=0.1V).

6.2.1. 0.18 MeV: Low irradiation energy

Effect of radiation fluence on C-V curve

Contrary to chapter 3, several irradiated MOS capacitors have been measured. Measured C(V) curves are shown in [Fig 6.2], which have been extracted for fluences up to $5 \cdot 10^{13}$ cm^{-2}. Above this fluence, no C(V) extraction was possible. It is suggested that this impossibility could be due to a very high negative gate voltage needed for entering into the accumulation regime (probably lower than -35V which is out of the measurement range). After

irradiation, the flatband voltage shifted toward negative values as indicated in [Table 6.2]. This shift indicates that irradiation induced the generation of additional oxide charges.

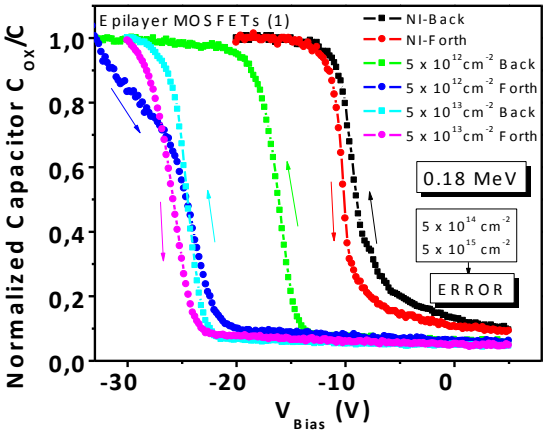


Fig 6.2. Normalized capacitance, hysteresis variation of non-irradiated and irradiated MOSFET (1) at 0.18 MeV following different fluences ($5{\cdot}10^{12}$ cm^{-2}, $5{\cdot}10^{13}$ cm^{-2}, $5{\cdot}10^{14}$ cm^{-2}).

The large hysteresis observed at F=$5{\cdot}10^{12}$ cm^{-2} also indicates an increase of ion mobile and interface trap charges. The oxide breakdown voltage and the oxide thickness do not seem to present any variation. At F = $5{\cdot}10^{13}$ cm^{-2}, a smaller ΔV_{FB} is observed than in the case of F = $5{\cdot}10^{12}$ cm^{-2}. A smaller hysteresis is obtained which means that a lower amount of ion mobile and interface trap charges is introduced in the MOS capacitance irradiated at F=$5{\cdot}10^{13}$ cm^{-2} during the measurement. However, the flatband voltage shift observed is more relevant. Indeed, the higher the fluence, the higher the amount of e-h pairs generated within the oxide, the more important the V_{FB} drift from the theoretical value (2.43V).

Energy (MeV)	Fluence (cm^{-2})	V_{FB}	ΔV_{FB}	$V_{\_Oxide\_Br}$	T_{ox}	N_{eff}	N_{fc}
0	0	-10.6	-0.9	28.3	42.5	1.2	5.5
0.18	$5{\cdot}10^{12}$	-17.4	-9.3	29.2	42.4	3.8	22.8
	$5{\cdot}10^{13}$	-25.6	-2.3	28.1	42.5	4.7	23.3
Unit		V	V	V	nm	$\times 10^{12}$ cm^{-2}	$\times 10^{9}$ cm^{-2}

Table 6.2. Electrical parameters extracted from the C(V) electrical characterization of NI and irradiated MOSFETs (1) at 0.18 MeV.

Effect of radiation fluence on transconductance curves

Fig. 6.3.a. shows the experimental I_{DS} (V_{GS}) curves for different fluence values. Contrary to what has been presented in chapter 3, there is no negative shift observed. According to what has been demonstrated before, we suggest that F_{TH} (the fluence value at which transconductance shift changes from negative to positive direction) should be lower than $5{\cdot}10^{12}$ cm^{-2}. The presented I_{DS} (V_{GS}) behavior indicates a predominance of acceptor-like interface traps

that continuously increase with fluence. A short general comment concerning the gate leakage current: For ***all irradiated MOSFETs*** at all energies and fluences, I_{GS} (V_{GS}) didn't show any leakage at room temperature. In some cases, the leakage current only started to be observed at 250ºC.

In comparison with NI MOSFETs, and despite of a smaller drain current capability (see annex [Fig. A.6.2.b]), μ_{fe} at V_{GS}=12V of irradiated MOSFETs at F=5·10^{12} cm^{-2} slightly increases [Fig 6.3.b]. Moreover, the μ_{fe} slope after reaching the maximum μ_{fe} value is less tilted in the case of the irradiated MOSFET at F=5·10^{12} cm^{-2}, which could be related with a smaller increase of the surface flatness. When irradiated at F=5·10^{13} cm^{-2}, μ_{fe} obtained presented acceptable values at V_{GS}=12V, being slightly lower than that of NI MOSFETs. However, when F > 5·10^{13} cm^{-2}, all the electrical parameters start to collapse, although the gate leakage current does not increase. The D_{it} profile above the valence band is plotted on [Fig A.6.3] together with the I_{DS} (V_{DS}) curves. As it can be seen, D_{it} is one order of magnitude higher at F=5·10^{14}cm^{-2} than in all the other cases. This study allowed observing the robustness limit of the irradiated MOSFETs with an oxynitrided gate oxide and phosphorus counter doping: For a proton irradiation at 0.18 MeV, we can guarantee that MOSFETs (1) can reliably operate as long as the absorbed fluence does not overcome 5·10^{13} cm^{-2}. Above this value, the electrical performances are drastically reduced with a sudden collapse.

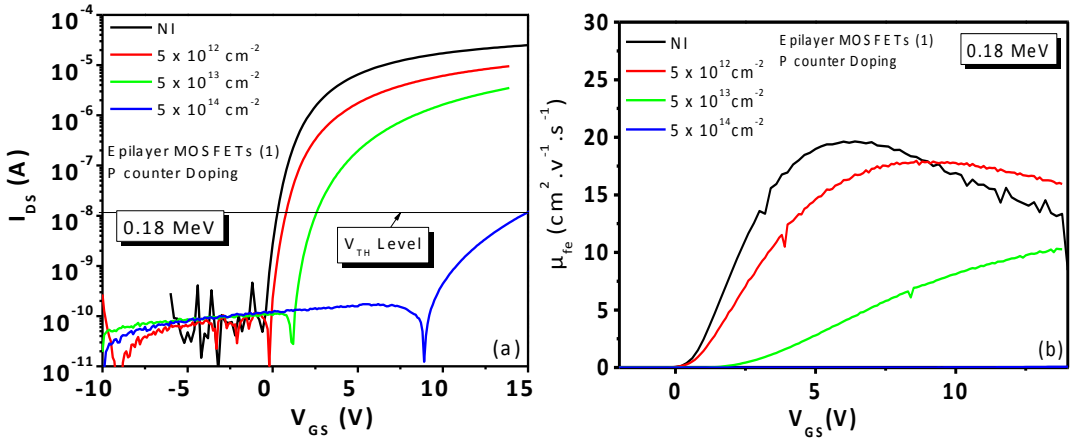


Fig 6.3. transconductance characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFET (1) at 0.18 MeV following different fluences.

Time bias stress analysis

The I_{DS}(V_{GS}) analysis performed under BSI stress allowed observing an important phenomenon: The observed GIDL after a positive gate bias stress decreased with the increase of the irradiation fluence, and is totally eliminated after a proton irradiation at F=5·10^{13} cm^{-2} [Fig A.6.4]. This is due to the acceptor predominance introduced by the irradiation process. With a positive stress bias, electrons at surface might be quickly trapped by the additional acceptor-like traps generated by irradiation, thus increasing V_{TH} and decreasing GIDL at the same time.

Up to a fluence of $5 \cdot 10^{13}$ cm^{-2}, the threshold voltage slowly raises [Fig A.6.5.a], and it drastically increases when $F > 5 \cdot 10^{13}$ cm^{-2}. However its time variation after a NBS remains quite stable. The ΔV_{TH} time stability of irradiated MOSFETs at fluences up to $5 \cdot 10^{13}$ cm^{-2} has been improved [Fig A.6.5.b] compared to NI MOSFETs. Its amplitude remains nearby 0V, meaning that almost no additional N_{it} or N_{ox} is generated at the SiO_2/SiC interface due to the BS time. Above $5 \cdot 10^{13}$ cm^{-2}, the ΔV_{TH} time stability and its amplitude start to be worse than that of the NI MOSFETs, because the amount of generated interface state charges starts to be significantly high so that ΔV_{TH} stability cannot be guaranteed. These additional results have shown the maximum proton fluence that MOSFETs (1) can receive at irradiation energy of 0.18MeV without degradation with bias stress time. Thus, the recovery effect can now be studied.

Post irradiation annealing

Post-irradiation annealing has be performed at 120ºC during 14 h and 90 h. BSI measurement has been performed after each annealing step. At the end of the last BSI measurement, BTI measurement has been performed.

Effect on C(V) capacitance

Post-irradiation annealing processes performed on the MOS capacitors didn't allow to observe any clear C(V) curve [Fig A.6.6.a]. Instead, a strange curve shape has been obtained on all measured capacitors. Thus no interpretation of the result could have been given.

Effect on μ_{fe}

At V_{GS} = 12V, all irradiated MOSFETs with fluences up to $5 \cdot 10^{13}$ cm^{-2} have shown a small recovery tendency [Fig 6.4.a]. However this recovery is quite small and does not seem to progress with long annealing times.

Time bias stress analysis

PIA MOSFETs irradiated at $F=5 \cdot 10^{12} cm^{-2}$ have decreased their V_{TH_NBSI} values below the NI one while keeping the time stability [Fig 6.4.b], although this variation is small. Indeed, the difference between the NI values and the one after 104h of N_2 annealing is about 0.5V. This means that PIA not only allowed a V_{TH} recovery but also it slightly changed the predominance of interface traps type from acceptors to donors. This phenomenon wasn't expected because it didn't occur in the case of MOSFETs#1 and MOSFETs#2 [see chapter 3 or 4]. Two hypotheses can be established to justify such a behavior:

1→ It could be related to the phosphorus counter doping. P could tend to move after an irradiation fluence of $5 \cdot 10^{12} cm^{-2}$ and annealing process and, as a result, some changes in the interface traps type predominance can happen. However, the diffusion of P is very low in SiC.
2→ During the irradiation process, electrons are trapped within the oxide bulk. In addition to the e-h recombination, the annealing process could induce an electron detrapping. These electrons can be tunneled from the oxide to the epilayer if not recombined, thus lowering V_{TH}.

At $F=5 \cdot 10^{13}$ cm^{-2}, the annealing didn't show any effect on the V_{TH_NBSI}. Indeed after 3600s of negative bias stress, V_{TH_NBSI} value of the post irradiation annealed MOSFETs was exactly the same as before the PIA [Fig A.6.8.b]. Thus, no significant change has been brought by the PIA. Although a clear V_{TH_NBSI} recovery tendency is observed on post-irradiation annealed MOSFETs irradiated at $F = 5 \cdot 10^{14} cm^{-2}$, its value is still above 10V [Fig A.6.8.c]. As shown in [Fig A.6.9], ΔV_{TH} of PIA MOSFETs irradiated at $F = 5 \cdot 10^{12} cm^{-2}$ and $5 \cdot 10^{13} cm^{-2}$ remain identical to that after the irradiation process in terms of time stability and amplitude.

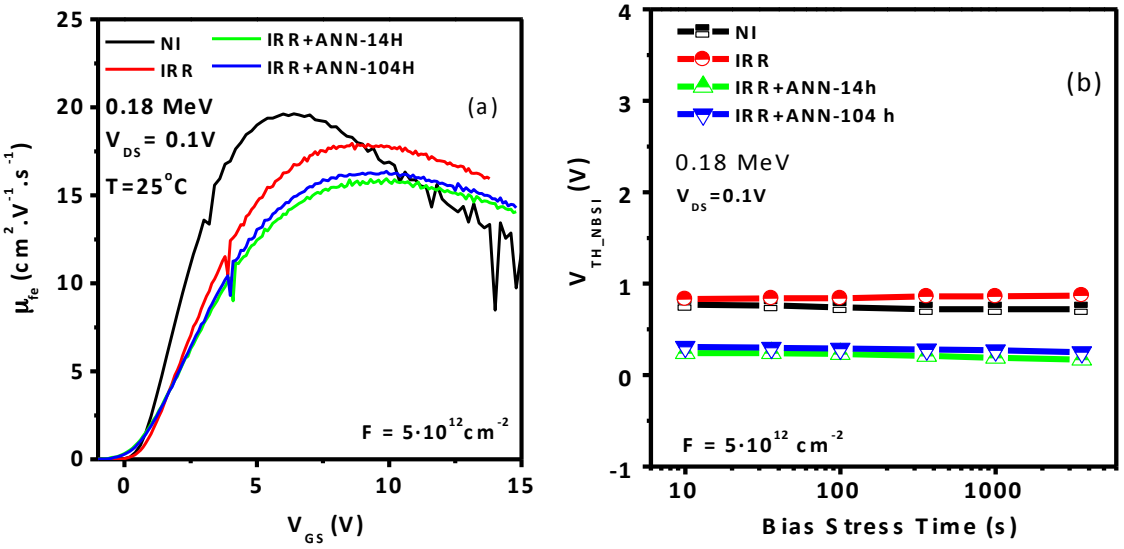


Fig 6.4. The field effect mobility time evolution (a) and the threshold voltage time evolution after a negative bias stress (b) for 0.18 MeV proton irradiated MOSFET (1) at $5 \cdot 10^{12}$ cm^{-2} and after several post irradiation annealing time (14h, 104h).

Post irradiation temperature annealing

A global comment regarding the measurement set up is that, in order to avoid any deterioration of the irradiated MOSFETs, the bias temperature analysis has been performed in the temperature range of [25ºC ; 250ºC] without overcoming 250ºC. As the number of irradiated component is limited, it has been decided to not take the risk of measuring at temperature higher than 250ºC.The time bias stress instability at 200ºC analysis has only been performed on one MOSFET (1), and the rest of MOSFET types will be tested in future works.

Effect on μ_{fe}

A general comment is that up to 200ºC, the irradiation effect at V_{GS}>12V is completely hidden by the roughness scattering [Fig A.6.10]. The irradiation effect is even not visible at 250ºC on MOSFETs irradiated at F = $5{\cdot}10^{12}$ cm^{-2}. At F = $5{\cdot}10^{13}$ cm^{-2}, the irradiation effect starts to be visible at 250ºC. As a consequence, there is a drastic decrease of the μ_{fe} with the increase of V_{GS} after the μ_{fe} peak value was reached. As a consequence, the temperature is high enough to strengthen other scattering mechanisms than that of the surface roughness, contributing to further μ_{fe} degradation.

Effect on V_{TH}

V_{TH} of PIA MOSFETs irradiated at F = $5{\cdot}10^{12}$ cm^{-2} starts to be negative at T = 50ºC. The behavior observed seems to follow the same tendency as the NI MOSFETs [Fig 6.5]. As seen from this figure, V_{TH} starts decreasing, reaching a minimum value before increasing very slightly. Thus for high temperature operation, this irradiation process is not suitable since the device is having a normally-on behavior. However, MOSFETs irradiated at F = $5{\cdot}10^{13}$ cm^{-2} do not shown a normally-on behavior. Indeed, the high temperature analysis has shown positive V_{TH} even at T=250ºC. The observed behavior is similar to that of other MOSFETs types (with other gate oxide), with a V_{TH} decreasing tendency when the temperature increase up to 200ºC before starting to increase again (see section 3.4.6). Consequently, the irradiation process, which has shown strong visible impact on the SiO_2/SiC interface, didn't act on the decreasing-increasing tendency of the V_{TH} with temperature. Thus, the optimum irradiation fluence that can guarantee a normal operation of MOSFET(1) for temperature up to 250ºC is founded to be within the range of [$5{\cdot}10^{12}cm^{-2}$; $5{\cdot}10^{13}$ cm^{-2}].

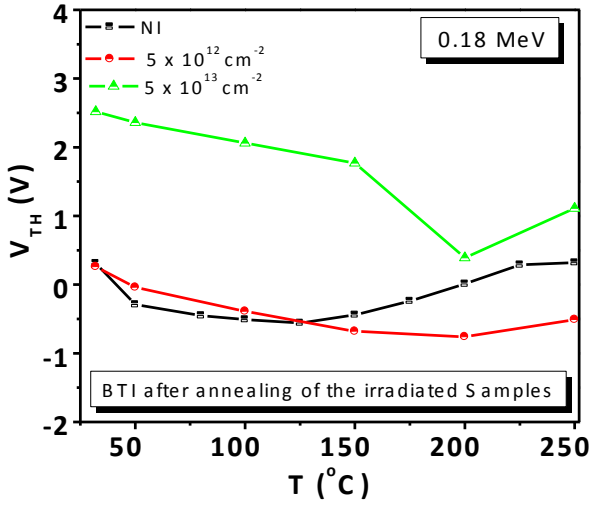


Fig 6.5. The V_{TH} temperature evolution for the NI MOSFET and post irradiation annealed MOSFET (1) of fluences of $5{\cdot}10^{12}cm^{-2}$ and $5{\cdot}10^{13}$ cm^{-2} at a proton irradiation of 0.18 MeV.

6.2.2. 10 MeV: High irradiation energy

Effect of radiation fluence on C-V

Only C(V) characteristics of samples irradiated at a fluence of $5 \cdot 10^{12} cm^{-2}$ could be measured, following the same behavior as the one observed for low irradiation energy in section 6.2.1. MOS capacitances irradiated at fluences above $5 \cdot 10^{12}\ cm^{-2}$ didn't show any results: All the measured curved had a noise-like shape. The negative flatband voltage shift can be seen in Fig A.6.12. However, contrary to the low irradiation MOS capacitance at 0.18 MeV, the flatband voltage hysteresis is even smaller than that of the NI samples [Table 6.3]. The fact of having narrower ΔV_{FB} than that of the NI samples does not predict that the amount of N_{eff} or N_{fc} will be lower since the flatband voltage shift with respect to the theoretical one (in our case 2.48V).

Energy (MeV)	Fluence (cm^{-2})	V_{FB}	ΔV_{FB}	$V_{\_Oxide\_Br}$	T_{ox}	N_{eff}	N_{fc}
0	0	-6.2	-0.5	28.3	42.5	0.7	4.1
10	$5 \cdot 10^{12}$	-7.7	-0.2	28.9	42.5	1.0	4.7
Unit		V	V	V	nm	$\times 10^{12}\ cm^{-2}$	$\times 10^{9}\ cm^{-2}$

Table 6.3. Electrical parameters extracted from the C(V) electrical characterization of NI and irradiated MOSFETs (1) at 10 MeV.

Effect of radiation fluence on transconductance curves

The irradiation effect is exactly similar to the one observed in chapter 3 in the case of a low proton fluence (section 3.4.1). The I_{DS} (V_{GS}) curves are represented in Fig 6.6.a. In this case, the threshold fluence F_{TH} that changes the predominant type of interface traps is $5 \cdot 10^{13}$ cm^{-2}. However for such fluence, the MOSFET is normally-on due to its negative V_{TH} value. A normally-off behavior is obtained on irradiated MOSFETs at a fluence of $5 \cdot 10^{14}\ cm^{-2}$. The μ_{fe} observed in irradiated MOSFET at $F = 5 \cdot 10^{12}\ cm^{-2}$ is higher by 20% at V_{GS}=15V when compared to the NI MOSFETs (see Fig 6.6.b). However, for MOSFETs irradiated at $5 \cdot 10^{12}\ cm^{-2} > F > 5 \cdot 10^{14}\ cm^{-2}$, high field μ_{fe} is practically equal to that of the NI MOSFETs, although they presented higher μ_{fe} peaks at lower V_{GS} values. The D_{it} values are approximately identical to that of the NI ones: They seem to slightly increase with the increase of F [Fig A.6.14.a].

Time bias stress analysis

Transconductance curves of the irradiated and non-irradiated MOSFETs are shown in [Fig 6.7]. We globally observed a similar decrease of the GIDL with the fluence increase as previously shown. This GIDL decrease has been observed in the case of all irradiated MOSFETs at all energies. This observation leads to the conclusion that proton irradiation process can be used for decreasing GIDL. Irradiated MOSFETs at all fluences have shown acceptable time stability

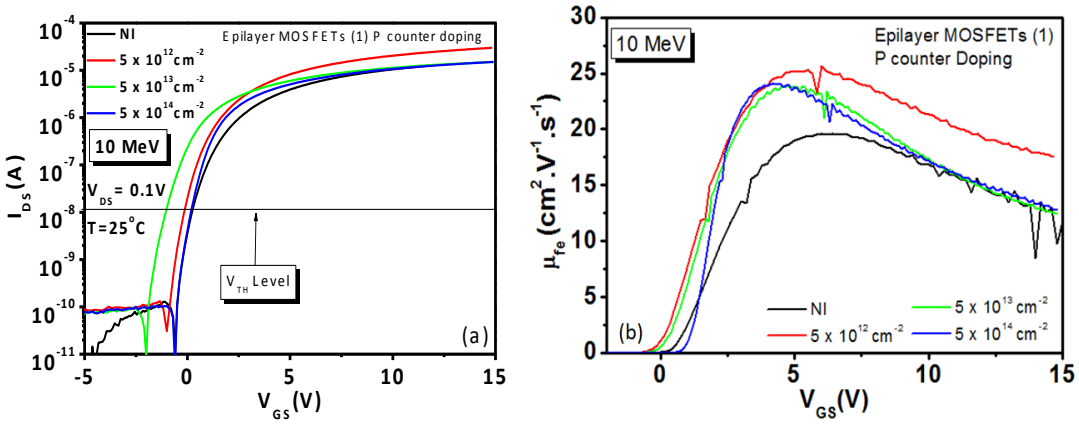


Fig 6.6. Transconductance characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFET (1) at 10 MeV following different fluences.

[Fig A.6.16], with a V_{TH_NBSI} and ΔV_{TH} time drift between the first stress and the last one at t=3600 lower than 0.3V. In addition, at the highest irradiation fluence, the threshold voltage hysteresis is the smallest. Another conclusion that can be drawn is that if the fabricated MOSFETs show a normally-on behavior, a high fluence irradiation treatment can be used for getting out of the normally-on zone, increasing the V_{TH} to the desired value (that depends on the irradiation fluence) while keeping its time stability and even decreasing its ΔV_{TH}.

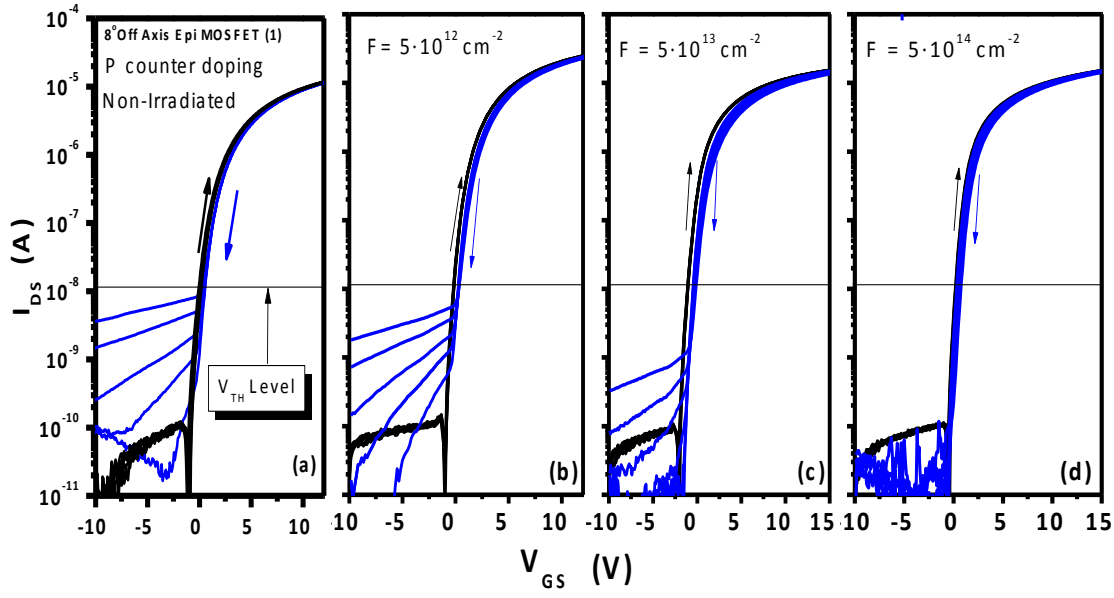


Fig 6.7. BSI Transconductance characteristic of MOSFET (1) non-irradiated (a) and irradiated at $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c), $5{\cdot}10^{14}$ cm^{-2} (d) with a 10MeV proton beam.

Post irradiation time annealing

Effect on μ_{fe}

Post irradiation annealing, in a general manner, induced a μ_{fe} recovery at all irradiated fluences as shown in Fig 6.8.a. MOSFETs irradiated at $5{\cdot}10^{13}$ cm^{-2} could not be measured after a 104h PIA since gate oxide was breakdown at V_{GS}=2V. Moreover, all irradiated MOSFETs at $5{\cdot}10^{13}$ cm^{-2} having identical geometrical parameters and transconductance characteristics didn't work after this PIA and, consequently, no BSI and BTI results could have been shown.

Time bias stress analysis

Generally, as observed in the case of the PIA impact on μ_{fe}, a V_{TH_NBSI} global recovery has been observed in [Fig 6.8.b] and in [Fig A.6.18] for PIA MOSFETs irradiated at fluences up to $5{\cdot}10^{13}cm^{-2}$. On the contrary, V_{TH_NBSI} values of PIA MOSFETs irradiated at $5{\cdot}10^{14}$ cm^{-2} increased after the PIA process. This might be due to an increase of charge trapping/detrapping effect leading to an increase of the negative charge within the oxide (an increase of V_{TH}) compared with the other irradiated MOSFETs at lower fluence values. At this fluence, the long annealing time didn't show any impact on the V_{TH_NBSI} shift after the first shift is observed. In all irradiated fluences, ΔV_{TH} didn't shown significant variation in both amplitude and time stability, being approximatively equal to that of before the PIA process [Fig A.6.19].

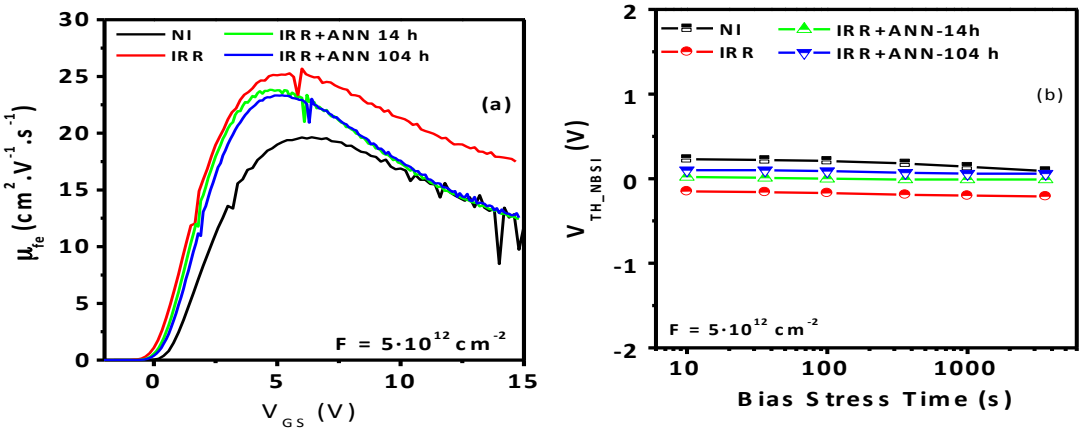


Fig 6.8. (a) The field effect mobility time evolution with the gate voltage and (b) the threshold voltage time evolution after a negative bias stress for 10 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2}, after irradiation and several post irradiation annealing time (14h, 104h).

Bias Temperature Instability Impact

BTI analysis have been performed on PIA MOSFETs irradiated at $5{\cdot}10^{12}cm^{-2}$ and $5{\cdot}10^{14}cm^{-2}$. μ_{fe} has a similar behavior to that of NI MOSFETs, although μ_{fe} peaks are higher [Fig. A.6.20]. Furthermore, μ_{fe} does not collapse at 250ºC for any of the PIA MOSFETs irradiated at $5{\cdot}10^{12}cm^{-2}$ and $5{\cdot}10^{14}cm^{-2}$. In addition, V_{TH} values are slightly different although the temperature behavior remains the same [Fig. A.6.21].

6.2.3. Conclusion on irradiated epitaxied MOSFETs with oxynitrided gate and phosphorus surface counters doping

MOSFETs with phosphorus counter doping and improved oxynitrided gate oxide have shown acceptable irradiation harshness behavior. However this behavior is quite depending on the irradiation energy that is received.

Conclusion on the 0.18 MeV irradiated MOSFETs: Good irradiation harshness is observed when the MOSFETs are irradiated up to a fluence of $5 \cdot 10^{13} cm^{-2}$. Higher irradiation fluence drastically decreases the device EP. Moreover, the ΔV_{TH} observed was very close to 0 V, and its time stability was even better than that of the NI MOSFETs. In addition, time and temperature PIA didn't show a significant recovery, except for MOSFET irradiated at $5 \cdot 10^{14} cm^{-2}$. In this case we suggest that an optimum irradiation fluence to slightly improve the device EP is $5 \cdot 10^{12}$ cm^{-2}.

Conclusion on the 10 MeV irradiated MOSFETs: Generally, the μ_{fe} peak slightly increased after irradiation, but its value at high field remains the same as the one before irradiation. PIA induced small recovery of the main EP and didn't impact the ΔV_{TH} amplitude and time stability. Irradiation at high fluence ($F = 5 \cdot 10^{14}$ cm^{-2}) provokes small increase of V_{TH} without impacting neither the MOSFET V_{TH} time stability nor its μ_{fe} value at low and high field. Thus such an irradiation process together with a PIA treatment might be useful for slightly increasing the V_{TH} value and getting out of the normally-on zone.

Globally, this study allows observing a decrease of the GIDL value together with the irradiation fluence increase. Moreover, no consequent gate leakage currents have been detected after irradiation. These gate leakage starts to exist at 250ºC. Finally, the irradiation robustness of MOSFETs with phosphorus counter doping and improved oxynitrided gate oxide has been shown, and the irradiation fluence limit for optimizing the main EP has been given.

6.3. 8º Off axis aluminum implanted MOSFETs with oxynitrided gate oxide

This set of transistor is built on implanted p-well (as in a VDMOS), instead of a P epilayer as usually used for optimization. It is worth mentioning that the μ_{fe} is typically lower on an implanted p-well.

6.3.1. 0.18 MeV: Low irradiation energy

Effect of radiation fluence on C-V

It was impossible to obtain reliable results about C-V measurements, thus any data on D_{it} could be obtained. However it does not really matter since, in MOSFETs (2) μ_{fe} can give directly an idea about the SiO_2/SiC interface quality.

Radiation effect fluence on transconductance curves

The observed effect of the fluence increase on the transconductance shift [Fig 6.9.a] is the same to the one reported in the (section 6.2.2), $F_{TH} = 5{\cdot}10^{12}\,cm^{-2}$ in this case. As observed in the case of irradiated MOSFETs (1), above an irradiation fluence of $5{\cdot}10^{13}cm^{-2}$, the EP collapse (V_{TH} > 25V; μ_{fe} at V_{GS} = 15V is inferior to 0.1V and $I_{D\_SAT\_MAX}$ < 1nA at V_{GS}=12V). As noted previously in chapter 3, a μ_{fe} increase of 30% has also been observed after an irradiation at F = $5{\cdot}10^{12}\,cm^{-2}$ [Fig 6.9.b]. However, above this fluence, μ_{fe} starts to decrease drastically. Consequently, not only V_{TH} starts increasing but also μ_{fe} decreases.

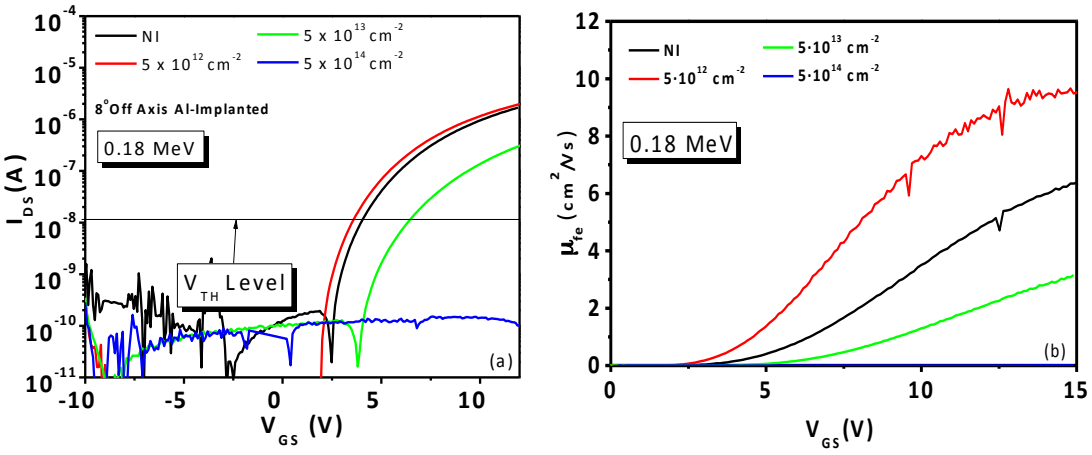


Fig 6.9. Transconductance characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFET (2) at 0.18 MeV following different fluences.

Time bias stress analysis

Time BSI analysis has shown identical I_{DS} (V_{GS}) behaviour [Fig B.6.25] as the one observed in section 6.2.1. V_{TH_NBSI} stability of the irradiated MOSFETs didn't change in comparison with the NI MOSFETs, and irradiated MOSFETs didn't show any significant amplitude time variation, its ΔV_{TH} being close to 0V with a small time drift [Fig B.6.26]. This first analysis demonstrates the irradiation robustness of a p-implanted MOSFET and its operation limits that are reached when $5{\cdot}10^{12}cm^{-2} < F < 5{\cdot}10^{13}\,cm^{-2}$.

Post irradiation time annealing

Effect on μ_{fe}

As in section 6.2.1, the adapted behavior of the μ_{fe} recovery of irradiated MOSFETs at $5{\cdot}10^{13}\,cm^{-2}$ and at high V_{GS} is very small. At lower fluence, no recovery is observed [Fig B.6.27].

Time bias stress analysis

The PIA process didn't impact the V_{TH_NBSI} and ΔV_{TH} time stability [Figs B.6.28 and B.6.29]. However it induced a recovery of the mentioned parameters [Fig 6.10.b] without impacting neither gate leakage current nor GIDL in all the cases, accounting for e-h recombination predominance over all the other mentioned effects in section 3.4.6.

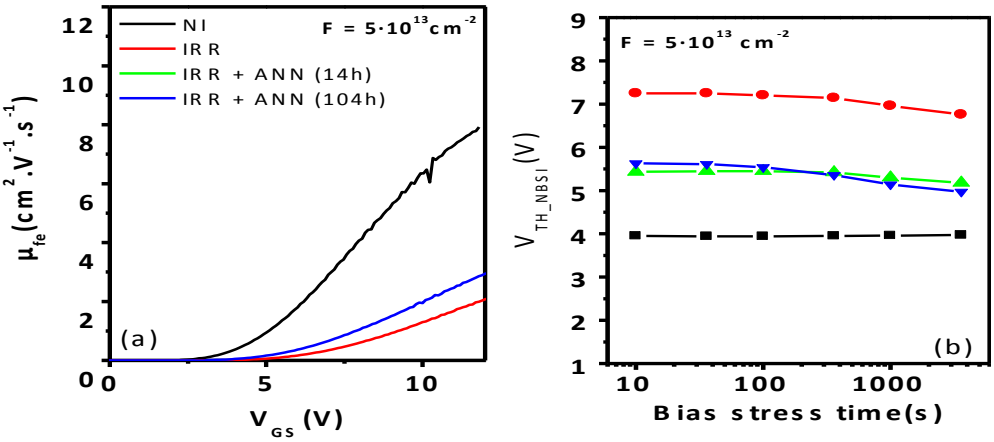


Fig 6.10. (a) The field effect mobility time evolution and the threshold voltage time evolution after a negative bias stress (b) for 0.18 MeV proton irradiated MOSFET (2) at $5{\cdot}10^{12}$ cm^{-2} and after several post irradiation annealing time (14h, 104h).

Post irradiation temperature annealing

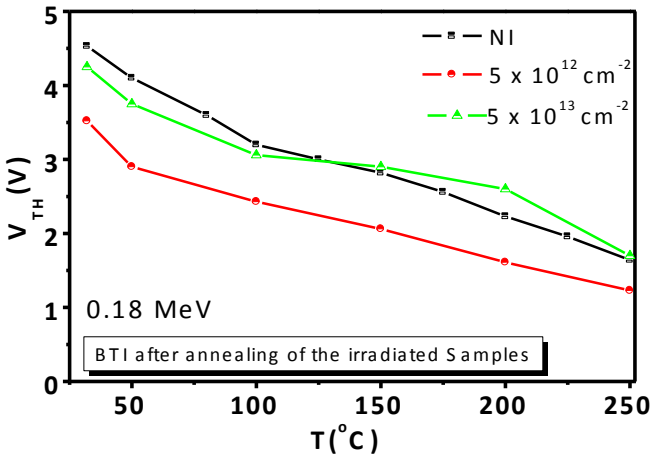
Effect on μ_{fe}

At high V_{GS} values, the μ_{fe} behavior at the lowest irradiated fluence is identical to that of previous observed ones: Above 150ºC, all the μ_{fe} values of NI and PIA MOSFETs tend to converge to a similar value, demonstrating the roughness scattering predominance [Fig B.6.30]. However, the difference, in this case, is that for irradiated MOSFETs at $F=5{\cdot}10^{12}cm^{-2}$, the μ_{fe} peak at low V_{GS} and at T=250ºC is higher by 47% than that of the NI MOSFET. Once the peak is reached, there is a clear trend tendency to the convergent value. Nevertheless, the robustness limit of such high temperature is reached when V_{GS} = 7.5V since the device failed. What is curious is that no leakage (no failed device) has been detected at 250ºC when the BTI test has been performed on a PIA MOSFETs irradiated at $F=5{\cdot}10^{13}cm^{-2}$. On the other hand, the μ_{fe} peak remained similar to that of the NI MOSFETs.

Effect on V_{TH}

In this case, the V_{TH} tendency was as expected: it decreases with increasing temperature [Fig 6.11]. No matter the irradiation fluence, the V_{TH} decrease is similar to that

measured on NI MOSFETs. Moreover, one effect has been observed that could be attributed to a recovery process: For the case of PIA MOSFETs irradiated at F = $5 \cdot 10^{13} cm^{-2}$, the V_{TH} at 25ºC is lower than that measured after the BSI stress. Indeed, due to the huge amount of MOSFETs that had to be measured with the BSI technique, the time difference between the BSI test carried out after the last PIA and the BTI stress was about 5 month. Thus, we suggest that, on such irradiated MOSFETs, a 5 month period at room temperature was enough to induce a V_{TH} recovery.



6.11. The V_{TH} temperature evolution for the NI MOSFET and post irradiation annealed MOSFET (2) of all fluences and doses at a proton irradiation of 0.18 MeV.

6.3.2. 10 MeV: High irradiation energy

Effect of radiation fluence on C-V

In this case, C(V) curves have been extracted [Fig 6.12], and it can be seen that the V_{FB} shift of the NI MOS capacitance is not so far from the theoretical value (-2.43V). Moreover, the high irradiation energy induced a small flatband voltage increase, and also reduces the ΔV_{FB}. However, the interface ledge zone is more important in the case of irradiated MOS at F = $5 \cdot 10^{13}$ cm^{-2} compared with the NI sample, accounting for an increase of fixed charges. The value of the

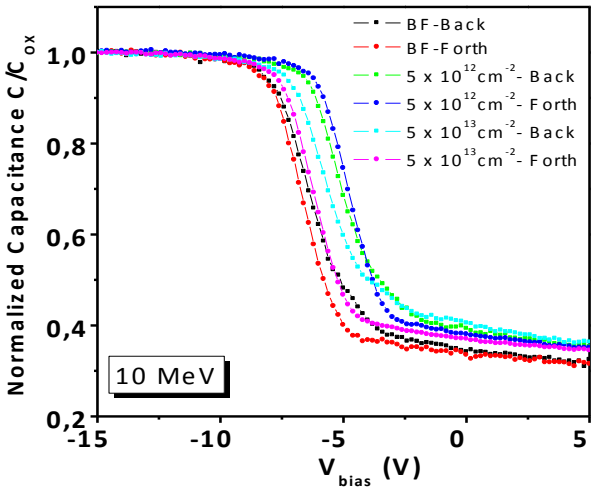


Fig 6.12. Normalized capacitance, hysteresis capacitance of non-irradiated and irradiated MOSFET (2) at 10 MeV following different fluences.

Energy (MeV)	Fluence (cm^{-2})	V_{FB}	ΔV_{FB}	$V_{\_Oxide\_Br}$	T_{ox}	N_{eff}	N_{fc}
0	0	-6.8	- 0.9	29.2	42.4	0.9	3.4
10	$5{\cdot}10^{12}$	-5.4	+ 0.2	29.3	42.3	0.6	3.1
	$5{\cdot}10^{13}$	-6.0	- 0.5	29.2	42.5	0.7	4.5
Unit		V	V	V	nm	$\times 10^{12}$ cm^{-2}	$\times 10^{9}$ cm^{-2}

Table 6.4. Electrical parameters extracted from the C(V) electrical characterization of NI and irradiated MOSFETs (2) at 10 MeV.

more important EPs is shown in Table 6.4. Identically, the gate oxide breakdown has not be impacted by the irradiation, no matter the irradiated fluence up to $5{\cdot}10^{13}cm^{-2}$. Above the mentioned fluence, C(V) analysis couldn't have been performed.

Effect of radiation fluence on transconductance curves

In this case, almost no impact of irradiation has been observed, in the sense that the transconductance curves almost overlapping each other [Fig 6.13.a]. I_{GS} (V_{GS}) of MOSFETs irradiated at all fluences didn't present any variation. As all the transconductance curves are similar, the μ_{fe} of the irradiated MOSFETs is also similar to that of the NI ones [Fig 6.13.b]. In addition, the observed D_{it} variation is in the same order of magnitude for all MOSFETs [Fig. B.6.34.a] but has been calculated at V_{DS}=0.1V. However, for higher V_{DS}, it seems that the irradiation impact is clearly visible and induces a decrease of the $I_{D\_SAT\_MAX}$ capability with the fluence increase.

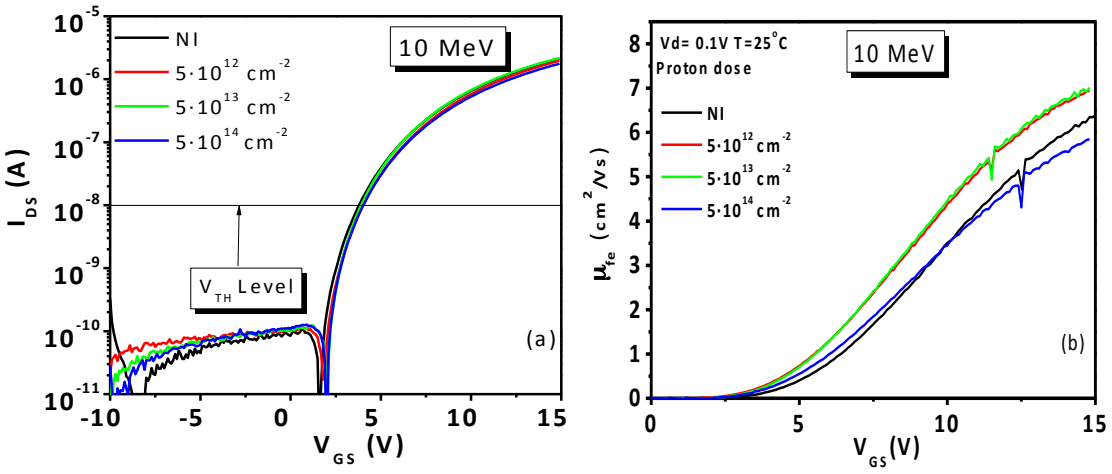


Fig 6.13. (a) Transconductance characteristics and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFETs (2) at 10 MeV following different fluences.

Time bias stress analysis

The V_{TH} time variation observed from the $I_{DS}(V_{GS})$ curves is similar to that of section 6.2.2, with a GIDL decrease after the irradiation process [Fig B.6.35] while keeping the V_{TH} time stability. The irradiation decreased the V_{TH_NBSI} amplitude by less than 1 V while keeping its time stability. In the worst case (irradiated MOSFET at F = $5{\cdot}10^{12}$ cm^{-2}), the ΔV_{TH} stability is identical to that of the NI MOSFET but with a lower amplitude. For higher fluences, the instability didn't occur. Thus, the stability has even been improved [Fig B.6.36].

Post irradiation time annealing

Effect on C-V curves

This is the only case where C(V) characteristics have been extracted after annealing [Fig B.6.37]. Generally, the annealing process didn't affect or didn't induce significant shift of the V_{FB}. Thus, its impact on the C(V) curve is negligible which is in accordance with the low irradiation impact on such a MOS device.

Effect on μ_{fe}

The effect on the μ_{fe} is irrelevant: A very small recovery has been observed for all PIA MOSFETs, accounting for a very low e-h recombination. These effects are represented on [Fig B.6.38]

Time bias stress analysis

V_{TH_NBSI} and ΔV_{TH} versus time are represented in Figs B.6.39 and B.6.40. For a fluence of F=$5{\cdot}10^{12}$ cm^{-2}, the amount of charge trapping/detrapping event that occurred due to the BSI

stress increases (section 6.2.2). In addition, the annealing process also increases positive charges within the oxide since V_{TH} decreases. However, PIA MOSFETs irradiated with higher fluences induced improved ΔV_{TH} stability. This might be due to a decrease of non-compensated oxide charge traps and ion mobile charges than in the case of BSI measurements on PIA MOSFETs irradiated at a fluence of $5 \cdot 10^{12}\,cm^{-2}$. Indeed, not all N_{it} and N_{ox} generated by the BSI are detected during the BSI measurement due to the fact that some of charges compensate to each-other within the oxide. Therefore two hypotheses are suggested to justify the ΔV_{TH} instability provokes by the annealing process on PIA MOSFETs irradiated at $5 \cdot 10^{12} cm^{-2}$ [Fig 6.14]

1) It seems that low irradiation fluences were enough to create a neutralized charge imbalance and, as a consequence, a V_{TH} shift during the BSI by e-h pair generation. However, with the fluence increase, the additional e-h generated within the oxide was high enough to reestablish the equilibrium between charges.

2) The oxide damage probability with low irradiation fluences is much lower than that of higher fluences. However this probability exists. With such high irradiation energy, the amount of damage in the gate oxide and in the epilayer is sufficiently important to generate critical gate oxide instabilities. This damage can even be enhanced by the annealing process due to the charge trapping/detrapping event that might predominated over the other mentioned phenomenon in section 3.4.6.

However, despite of the mentioned instabilities observed at $5 \cdot 10^{12} cm^{-2}$, they are not very critical since after post irradiation annealing ΔV_{TH} remains as stable as NI MOSFETs.

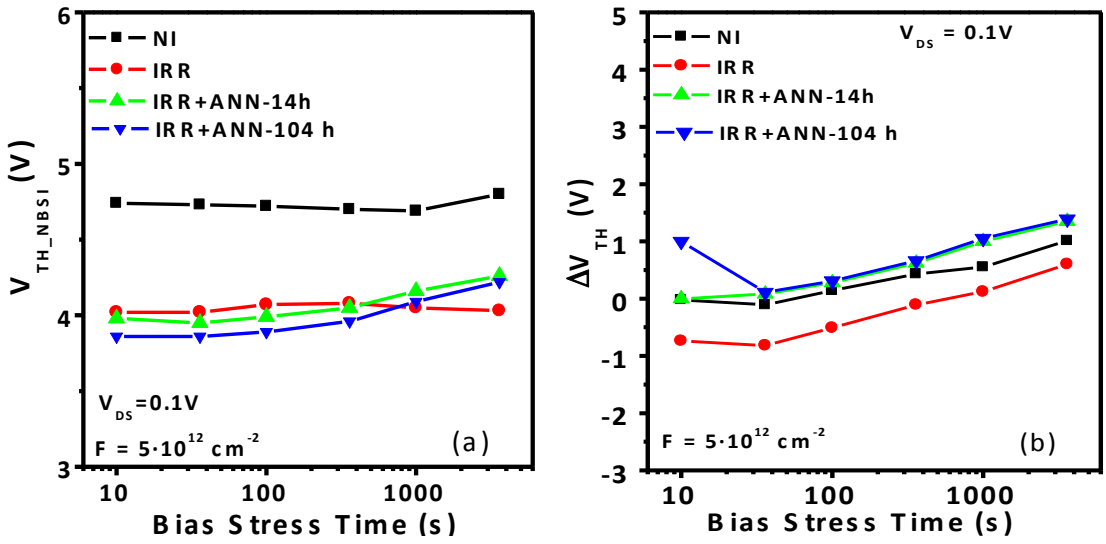


Fig 6.14. (a) The threshold voltage time evolution after a negative bias stress and the threshold voltage hysteresis time evolution (b) after a 10 MeV proton irradiated MOSFETS (2) at $5 \cdot 10^{12}\ cm^{-2}$ and after several post irradiation annealing time (14h, 104h).

Bias Temperature Instability Impact

Effect on μ_{fe}

In the case of PIA MOSFETs irradiated at F=5·10^{13} cm^{-2} and 5·10^{14} cm^{-2}, the observed μ_{fe} behavior is similar to what has been observed in section 6.3.1 as shown in [Fig B.6.41]. In the case of the BTI study on PIA MOSFETs irradiated at F=5·10^{12}cm^{-2}, a surprising high μ_{fe} peak has been detected at 250ºC [Fig B.6.41.b]. To our knowledge, this value of 62 cm^{2}V^{-1}s^{-1} has never been reported in the literature on p-type implanted nMOSFETs. Moreover, the important increase of μ_{fe} at 250ºC has already been identified in chapter 3 section 3.5.4.

Effect on V_{TH}

The behavior observed is similar to that of section 6.3.1. Results are shown in [Fig B.6.42]: V_{TH} decreases with increasing temperature.

6.3.3. Conclusion on irradiated 8º Off axis aluminum implanted MOSFETs with oxynitrided gate oxide

Conclusion on the 0.18 MeV irradiated MOSFETs: The existence of a threshold fluence that changes the amount of predominant interface charge traps from donors to acceptors is confirmed. For irradiated MOSFETs at F=5·10^{12}cm^{-2}, μ_{fe} has increased in comparison to the NI MOSFETs. A good V_{TH} time stability has been demonstrated after irradiation and PIA processes. Moreover, the recovery effect induced by the annealing process has been put in evidence. Nevertheless, long time PIA didn't seem to show more recovery than the one observed after a short time PIA. μ_{fe} peak at high temperature of PIA MOSFETs irradiated at 5·10^{12}cm^{-2} is much higher than that of the NI MOSFETs. In all the cases, V_{TH} decreases when increasing temperature. The fact that the gate oxide of MOSFETs (2) is similar to that of MOSFETs (1) enhance the conclusion previously established in section 3.4.6 that the abnormal V_{TH} variation observed in MOSFET(1) could be related to issues concerning the epilayer (screw dislocation, edge dislocation etc…) that might highly impact the device during the BTI measurement. Finally, the limit fluence for MOSFET (2) robustness with Al-implanted p-well is about 5·10^{13}cm^{-2}.

Conclusion on the 10 MeV irradiated MOSFETs: Very small shift of the transconductance curves and C(V) curves of MOSFETs irradiated at all fluences have been observed. Moreover, the PIA process didn't seem to critically influence the V_{TH} behavior and its hysteresis. BTI measurements allowed to put in evidence a surprising μ_{fe} peak of the PIA MOSFETs irradiated at F=5·10^{12} cm^{-2}, which is 4 times higher than that of the NI MOSFET.

This study allows observing that no real negative contribution on the GIDL and I_{GS} current is brought by the irradiation or by the PIA process. Some gate leakage starts to be detected around 250ºC. Finally, the irradiation robustness of an Al-implanted nMOSFETs with 8ºOff axis has been shown, and the irradiation fluence limit allowing a correct operation of the MOSFETs has been given. Thus, it might be relevant to see what can possibly be the irradiation impact on Al-implanted MOSFETs having a very flat (low roughness) SiO_2/SiC interface.

6.4. On-axis aluminum implanted MOSFETs with oxynitrided gate oxide

The same experiment has been repeated on on-axis aluminum implanted MOSFET. Before processing the surface has been polishing in order to completely eliminate the surface roughness. All the detail regarding the growth difficulties of an on-axis samples have been explained in the previous chapter (see section 5.2.2).

6.4.1. 0.18 MeV: Low irradiation energy

Effect of radiation fluence on C-V

Due to the impossibility of measuring the MOS capacitance for all irradiated devices at all energies, any relevant conclusion has been established.

Effect of radiation fluence on transconductance curves

Results observed in the case of irradiated MOSFET (3) present similar behavior to those of section 6.3.1 [Fig 6.15.a]. It seems that the irradiation at $F=5\cdot10^{14}\,cm^{-2}$ didn't impact MOSFETs (3) as much as it impacted MOSFETs (2). Indeed, at this fluence, V_{TH} of irradiated MOSFETs (3) is about 12.8V whereas in the case of irradiated MOSFETs (2), no I_{DS} current has been detected even at 15V [Fig 6.9]. Thus, the fact of having a MOSFET made on a complete flat substrate increases somehow the low energy high fluence radiation robustness. Although μ_{fe} values of irradiated MOSFETs (3) with a fluence of $5\cdot10^{12}\,cm^{-2}$ seemed to be slightly higher to that of the NI MOSFETs [Fig 6.15.b] by 4%, the maximum $I_{D\_Sat\_Max}$ value was founded to be 8% lower: These μ_{fe} values decrease drastically with the fluence increase, accounting for a clear negative impact of irradiation.

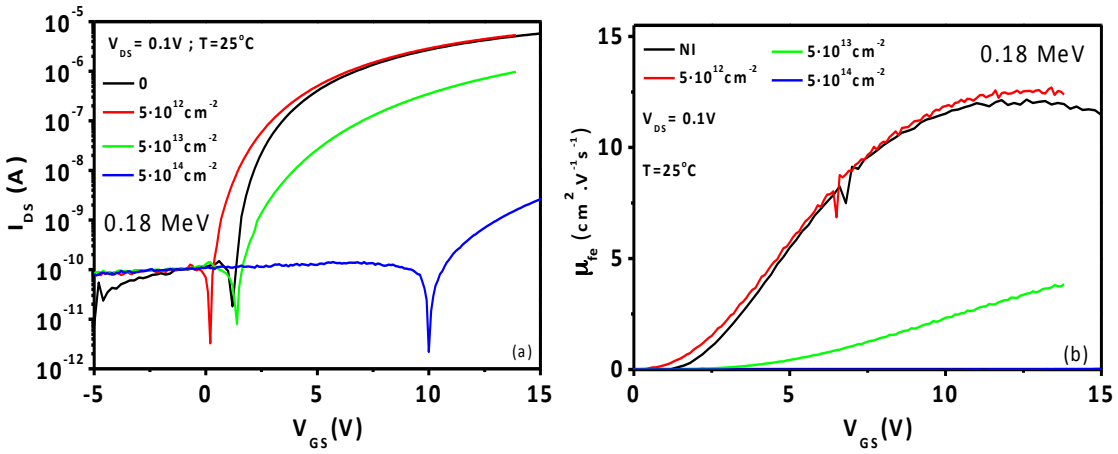


Fig 6.15. Transconductance characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFETs (3) at 0.18 MeV following different fluences.

Time bias stress analysis

I_{DS} (V_{GS}) results observed are similar as those of the section 6.2.1. With the increase of the proton fluence the GIDL current decreased and disappeared after F = $5 \cdot 10^{13} cm^{-2}$ [Fig C.6.45]. The V_{TH_NBSI} and ΔV_{TH} behaviors are also similar to 6.2.1: V_{TH_NBSI} is constant with time for all fluence while irradiated samples at F=$5 \cdot 10^{13}$ cm^{-2} have shown a decrease of its time stability due to the predominance of acceptor at the SiO_2/SiC interface [Fig C.6.46].

Post irradiation time annealing

Effect on μ_{fe}

The behavior obtained is similar to that of section 6.3.1: No change of the μ_{fe} values has been observed in PIA MOSFETs irradiated at $5 \cdot 10^{12}$ cm^{-2}, but a recovery did occur at $5 \cdot 10^{13} cm^{-2}$, as shown in [Fig 6.16.a]. However, this recovery does not progress after a long annealing time. In order to induce a more efficient recovery, an alternative solution would be to perform an annealing process at a higher temperature although configuration do not allow it.

Time bias stress analysis

The PIA effect on MOSFETs (3) V_{TH_NBSI} is also similar to that of section 6.3.1 as it can be seen from [Fig 6.16.b]. The annealing process didn't seem do have any impact on the ΔV_{TH} hysteresis [Fig C.6.49].

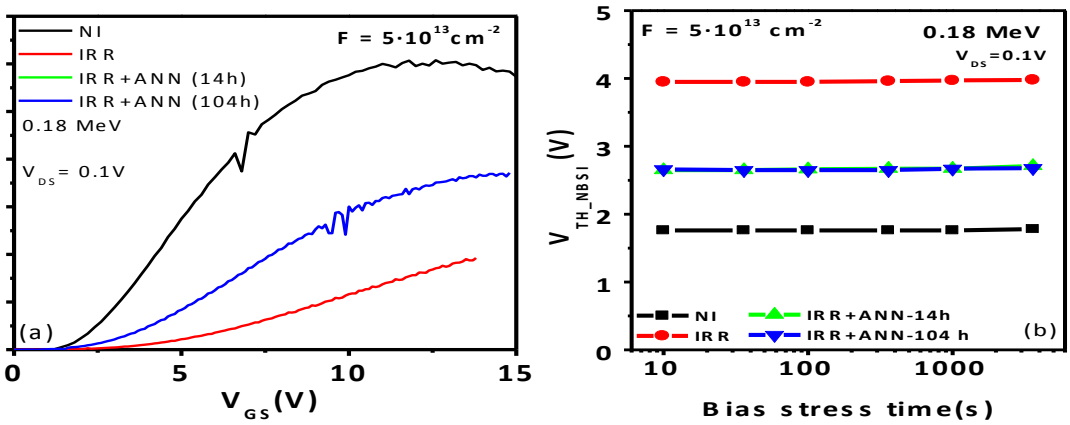


Fig 6.16. The field effect mobility time evolution (a) and the threshold voltage time evolution after a negative bias stress (b) for 0.18 MeV proton irradiated MOSFETS (3) at $5{\cdot}10^{13}$ cm^{-2} after irradiation and several post irradiation annealing time (14h, 104h).

Post irradiation temperature annealing

Effect on μ_{fe}

The high temperature behavior is different to what it was founded in the case of PIA MOSFETs (2). Generally, it seems that the oxide breakdown occurred at annealing temperatures between 200ºC and 250ºC at low V_{GS} for both PIA MOSFETs irradiated at $5{\cdot}10^{12}$ cm^{-2} and $5{\cdot}10^{13}$ cm^{-2}. PIA MOSFETs irradiated at F=$5{\cdot}10^{12}cm^{-2}$ presented similar μ_{fe} aspect as presented in section 6.3.1: at V_{GS} = 15V, all μ_{fe} above 100ºC seemed to tend to the same μ_{fe} value [Fig 6.50.b], whereas, in the case of the PIA MOSFETs irradiated at $5{\cdot}10^{13}cm^{-2}$, μ_{fe} is lower than the value of NI MOSFET [Fig C.6.50.c]. In general, above 100ºC-150ºC, all the μ_{fe} values of PIA MOSFETs studied in the frame of this thesis tend to the values of NI MOSFETs.

Effect on V_{TH}

There is a good agreement with results presented in section 5.2.3. V_{TH} decrease very slightly with the temperature, even for PIA MOSFETs irradiated at fluences up to $5{\cdot}10^{13}$ cm^{-2}. The variation in the case of the irradiated MOSFETs seems to follow the same tendency as the NI samples. Thus, the irradiation followed by the PIA process didn't show any impact on the V_{TH} behavior at high temperatures [Fig 6.17] However, as explained previously, it impacts the gate leakage current at temperatures higher than 200ºC.

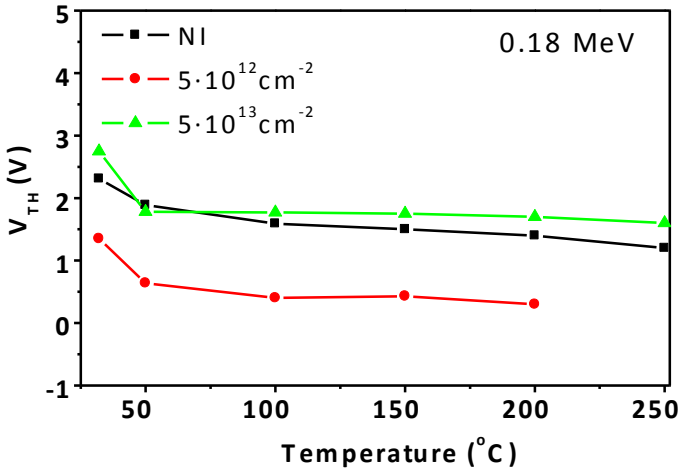


Fig 6.17. The V_{TH} temperature evolution for the NI MOSFETs and post irradiation annealed MOSFETs (3) of all fluences and doses at a proton irradiation of 0.18 MeV.

6.4.2. 10 MeV: High irradiation energy

Effect of radiation fluence on transconductance curves

We are in a similar case to the one observed for electron irradiation at 15 MeV (see chapter 4), where single event due to the collision probability could have occur. Indeed, at a low irradiation fluence ($5{\cdot}10^{12}$ cm^{-2}), an increase of the I_{DS} current capability has been founded, and is plotted in [Fig C.6.52.a]. However, an unexpected phenomenon occurred when the fluence increased: the amount of generated acceptor by irradiation at the SiO_2/SiC interface seemed to be lower in the case of irradiated MOSFETs at a fluence of $5{\cdot}10^{14}$ cm^{-2} in comparison with the ones generated at a fluence of $5{\cdot}10^{13}$ cm^{-2}. As a consequence, the V_{TH} positive shift difference between the irradiated MOSFET at $5{\cdot}10^{13}cm^{-2}$ (M1) and the NI MOSFET is superior to that of between the irradiated MOSFET at $5{\cdot}10^{14}cm^{-2}$ (M2) and the NI MOSFETs. To explain this peculiar shift which goes against what had been explained before, we suggest that despite of higher irradiation fluence, less collision occurred between the incident proton beam crossing M2

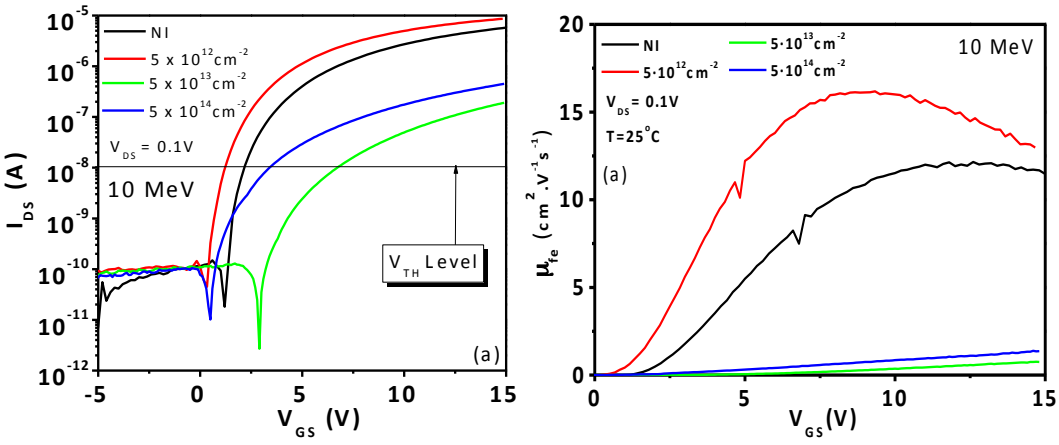


Fig. 6.18. Transconductance characteristics (a) and μ_{fe} (V_{GS}) of non-irradiated and irradiated MOSFETs (3) at 0.18 MeV following different fluences (b).

and its gate oxide than those occurring when the proton beam crossed M1. As the irradiation energy is very high, the collision probability is very low. Nevertheless, the possibility of having more impact when F = $5{\cdot}10^{13}$ cm^{-2} than when F = $5{\cdot}10^{14}$ cm^{-2} is not negligible, and this could explain the V_{TH} shift tendency. However, whether F = $5{\cdot}10^{13}$ cm^{-2} or $5{\cdot}10^{14}$ cm^{-2}, and despite of the mentioned explanation, we observed how critical is the impact of proton beam on such MOSFETs. The damage observed is so important in such a way that μ_{fe} does not exceed 1.5 $cm^2.V^{-1}.s^{-1}$, which is at least 9 times lower than that of the NI MOSFETs [Fig C.6.53.a].

In addition, the maximum drain saturation current at V_{GS} = 12V is more than two orders of magnitude lower than that of the NI MOSFETs. MOSFETs irradiated at a fluence of $5{\cdot}10^{12}$ cm^{-2} showed an increase of μ_{fe} peak in comparison with NI MOSFET, μ_{fe} values at V_{GS}=15V and its maximum saturation drain current being approximately 9% and 15% higher, respectively [Fig C.6.53.b]. Thus, before considering the BSI and BTI, an irradiation fluence of $5{\cdot}10^{12}$ cm^{-2} should be the optimum one, and the fluence limit allowing a small improvement of the electrical parameters of aluminum p-type implanted on-axis MOSFET (3). In the case of irradiated components at high energies, it seemed that 8º off-axis MOSFETs (2) with Al-implanted had best robustness that that of on-axis devices.

Time bias stress analysis

As in section 6.2, the increase of the irradiation fluence implied a GIDL MOSFETs decrease [Fig 6.19]. However, this decrease is really put in evidence when F ≥ $5{\cdot}10^{13}$$cm^{-2}$, which corresponds to the critical fluence that collapses the MOSFET EP, as previously described. The irradiation process didn't impact the V_{TH} time stability, as presented in [Fig C.6.55]. For the lowest irradiation fluence, the ΔV_{TH} amplitude became smaller than that of NI MOSFET, and its time stability has even been improved. Moreover, at such a fluence ($5{\cdot}10^{12}$ cm^{-2}), V_{TH} of the irradiated MOSFETs is slightly lower to that of the NI MOSFET. These facts

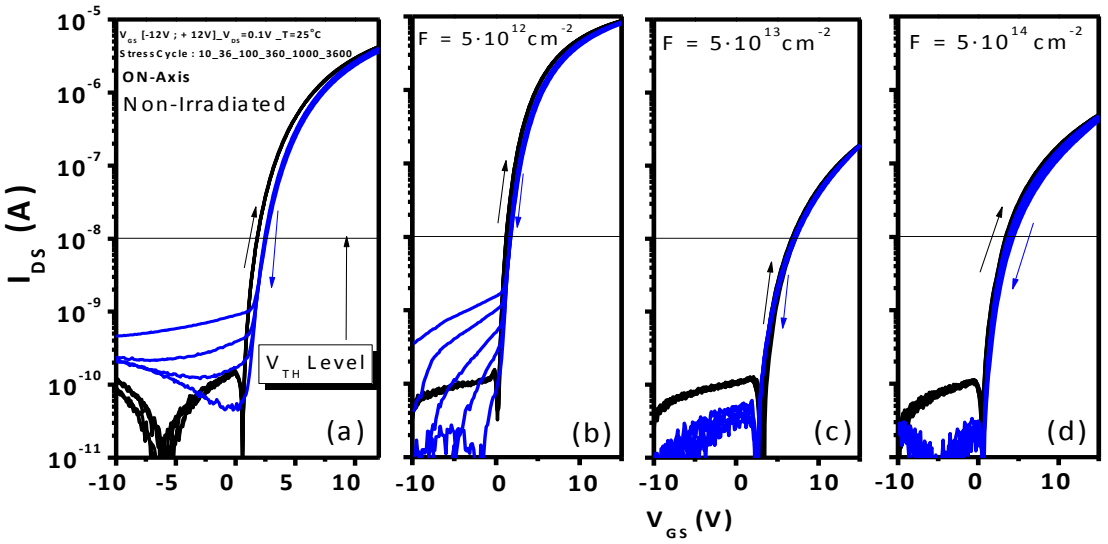


Fig 6.19. BSI Transconductance characteristic of MOSFETs (3) non-irradiated (a) and irradiated at 10 MeV with $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c) and $5{\cdot}10^{14}$ cm^{-2} (d) proton fluences.

account for a lower charge trapping/detrapping effect at the SiO_2/SiC interface. Therefore, we can conclude that, from the time stability point of view, high energy irradiation process at $5{\cdot}10^{12}cm^{-2}$ might be a suitable process for EP improvement of on-axis Al-implanted MOSFET.

Post irradiation time annealing

Effect on μ_{fe}

As observed in Fig C.6.56, PIA process on MOSFETs (3) presented two types of effects depending on the irradiation fluence: A complete μ_{fe} recovery has been observed on PIA MOSFETs irradiated at $5{\cdot}10^{12}cm^{-2}$: μ_{fe} (V_{GS}) PIA MOSFETs completely fit with the curve of NI MOSFETs [Fig 6.20.a]. For the other PIA MOSFETs irradiated at higher fluences, this recovery does not occur because the damage caused by the proton beam is high enough to prevent from its recovery, contrarily to the case of PIA MOSFETs irradiated at lowest irradiation fluence.

Time bias stress analysis

Two types of effects have been put in evidence in this case. For the two lowest fluences, the V_{TH} recovery seemed to occur after a long time annealing. In the case of PIA MOSFETs irradiated at $5{\cdot}10^{12}$ cm^{-2}, the PIA process almost induced a total V_{TH} recovery [Fig 6.20.b] that had been previously shown with the total μ_{fe} recovery. However, for PIA MOSFETs irradiated at $5{\cdot}10^{13}$ cm^{-2}, the V_{TH} recovery toward the NI MOSFET values is only partial but it really occurs [Fig C.6.57.b]. Moreover, at this fluence, the PIA process induced ΔV_{TH} instabilities [Fig C.6.58.b]. Secondly, it has been observed that PIA performed on irradiated MOSFETs at $5{\cdot}10^{14}$ cm^{-2} has increased the amount of acceptor-like traps at the SiO_2/SiC interface, implying

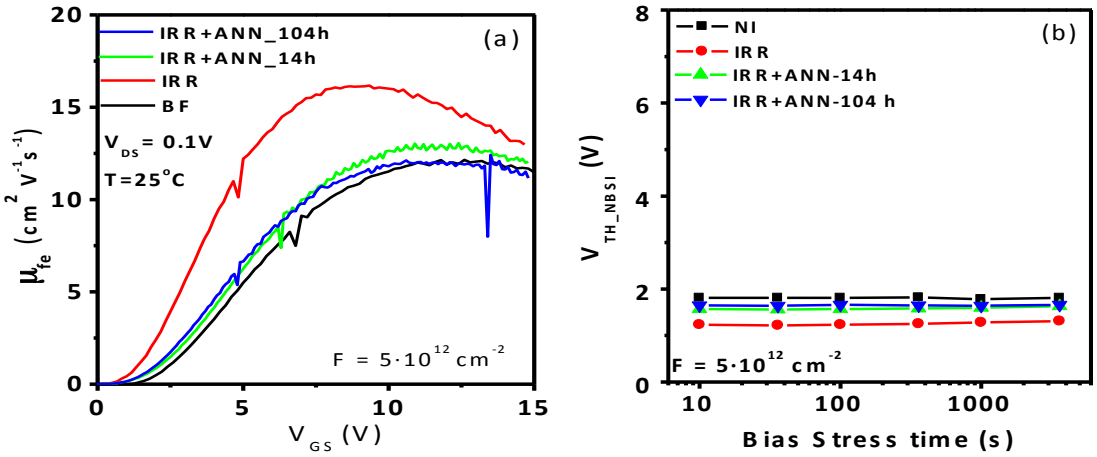


Fig 6.20. (a) The field effect mobility time evolution and (b) The threshold voltage time evolution after a negative bias stress for 10 MeV proton irradiated MOSFETS (3) at $5{\cdot}10^{12}$ cm^{-2} after irradiation and several post irradiation annealing time (14h, 104h).

an increase of V_{TH} [Fig C.6.57.c]. This is not easy to understand because for a fluence of $5{\cdot}10^{13}cm^{-2}$, the amount of acceptors generated by irradiation was higher, and it seems that the PIA process decreased this amount of acceptors whereas it had the contrary effect after a PIA process of a MOSFET irradiated at $5{\cdot}10^{14}cm^{-2}$. We previously mentioned that the damage at the SiO_2/SiC interface should be lower despite of high irradiation fluence, but any conclusion on this behavior can be provided. Perhaps the tunneling effect predominates over the other mechanisms mentioned in chapter 3.

Bias Temperature Instability Impact

Effect on μ_{fe}

BTI analysis performed on PIA MOSFET (3) irradiated at $5{\cdot}10^{12}$ cm^{-2} has shown the same tendencies described in section 6.2.2. In this case, the μ_{fe} peak is not observed at high temperature [Fig C.6.59.b], and, above 100ºC, μ_{fe} value at all temperatures and at V_{GS} = 15V tends, to similar values. Curiously, these values are similar to that of the irradiated MOSFETs(2) at the same fluence. Irradiated MOSFETs at fluences superior to $5{\cdot}10^{12}cm^{-2}$ have shown a clear decreasing tendency that depends on the irradiation fluence: The higher the irradiation fluence, the lower the μ_{fe} value at high temperature. Thus, at high irradiation energies, the "on-axis" parameter negatively affects the high temperature operation of PIA MOSFETs. Contrarily to the off-axis case, it seems the scattering mechanisms are significantly more severe at high irradiation energies, limiting the μ_{fe} value. In addition, it must be noted that NI MOSFETs (3) have, at high temperature, similar μ_{fe} values to those of NI MOSFETs (2). This is also true for MOSFETs (2) and (3) when the irradiation fluence does not overcome $5{\cdot}10^{12}cm^{-2}$. In terms of high temperature operation, the robustness limit of an implanted MOSFET 8º off-axis is higher to that of an on-axis one (which is limited to a fluence value of $5{\cdot}10^{12}cm^{-2}$).

Effect on V_{TH}

On-axis MOSFETs do not show a drastic drop of V_{TH} when increasing temperature [Fig C.6.60]. Note that in the case of off-axis MOSFETs the V_{TH} decrease was remarkably more important. The irradiation impact on V_{TH}, even at high temperatures, at all fluences globally did not compromise the device normally-off behavior.

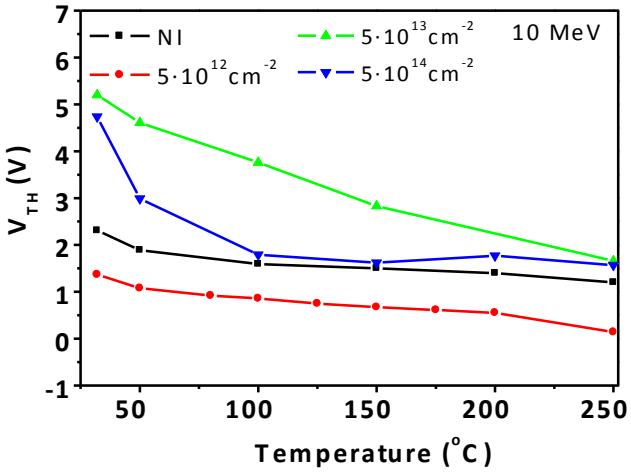


Fig 6.21. The V_{TH} temperature evolution for the NI MOSFETs and post irradiation annealed MOSFETs (3) of all fluences and doses at a proton irradiation of 10 MeV.

6.4.3. Conclusion on irradiated on-axis aluminum implanted MOSFETs with oxynitrided gate oxide

Conclusion on the 0.18 MeV irradiated MOSFETs: In addition with the μ_{fe} improvement with an irradiated dose of $5{\cdot}10^{12}cm^{-2}$, a positive point is that GIDL observed before irradiation also decreased with the fluence while keeping V_{TH_NBSI} constant with time. However, because the charge trapping predominates over the other mentioned effects at irradiated fluence superior to $5{\cdot}10^{12}cm^{-2}$, μ_{fe} collapse while GIDL decreases. BSI stress has shown similar V_{TH} and ΔV_{TH} to that of the previous section and the annealing process has shown a significant V_{TH} recovery at MOSFET irradiated at $5{\cdot}10^{13}cm^{-2}$. The BTI analysis revealed an oxide breakdown voltage between 200ºC and 250ºC, which is lower than that obtained in the previous case. Finally, the irradiation fluence limit that guaranteed a normal operation of the on-axis Al-implanted p-type nMOSFETs does not have to exceed $5{\cdot}10^{12}cm^{-2}$.

Conclusion on the 10 MeV irradiated MOSFETs: Although a general trend based on the EP evolution with the increase of the irradiation fluence could have been established, the study of this case allowed us to confirm that proton high-speed irradiation damage inside a MOSFET component also relies on collision probabilities. Indeed, $5{\cdot}10^{14}$ cm^{-2} irradiation impact on MOSFETs had been founded to be less critical than that of $5{\cdot}10^{13}$ cm^{-2}. In all the cases, irradiation at $5{\cdot}10^{12}$ cm^{-2} had shown improvement of the EP without altering neither the V_{TH} time

and temperature stability, nor the GIDL and gate source leakage before and after the PIA process. Moreover, the ΔV_{TH} is reduced and its time stability observed was better to that of the NI MOSFET. Therefore, the irradiation fluence of $5 \cdot 10^{12}$ cm^{-2} correspond to both the optimum fluence that induce an improvement of the EP and to the limit dose before the robustness start to collapse.

6.5. Conclusion

The proton irradiation and PIA impact on the 2nd MOSFETs studied in the previous chapter has been evaluated. As described, the average fluence limit tolerable by the MOSFETs having the optimized oxinitrided gate oxide will be around $5 \cdot 10^{12}$ cm^{-2}. This statement is independent of the MOSFETs structure. In addition, several remarkable conclusions could have been established:

- With the increase of the irradiation fluence, the drain leakage current in off-state decreased.

- A threshold fluence that changed the interface traps predominance from donor to acceptor with the fluence increase is, once again, put in evidence.

- The PIA process induced very small recovery, and, in most of the case, long time annealing does not affect the V_{TH} recovery.

- The BTI analysis allowed confirming that, in most of the cases, scattering mechanism predominated much more than the irradiation effect, due to the fact that the high temperature induce a e-h recombination that is much more efficient than the long time annealing at 120ºC. Moreover, in a specific case, a peak of μ_{fe}, similar to what had been observed in chapter 4 has been founded. This peak is not understood and is attributed to a single event.

- The curious V_{TH} decrease with the temperature increase observed in the case of the irradiated MOSFETs having an epilayer body is probably due to deep defect that are proper to the epilayer itself.

Non-Irradiated On-axis nMOSFETs has shown a much better behavior than that of non-irradiated Al-implanted 4H-SiC. However, the irradiation robustness at high energies is much better in the case of Al-implanted 4H-SiC 8º off-axis nMOSFETs.

To conclude, irradiation harshness of MOSFETs having oxynitrided gate oxide has been demonstrated and the limit of robustness had also been given. Nevertheless, a full understanding of the involved mechanisms under high temperature conditions is still required. In the next generation of components, further experiment remains to be performed. Among them the DLTS and XPS analysis should be the one that might help to identify the deep cause of the defects generated by irradiation mechanism.

General Conclusions

This work carried out in the framework of this Ph.D. Thesis dealt with the improvement of the 4H-SiC MOSFET p-well implantation and gate oxidation processes together with the study of the irradiation impact and robustness limit on the MOSFETs electrical parameters. Optimized fabrication processes have been developed and deeply detailed. In parallel, the impact of irradiation and post-irradiation annealing on MOSFETs having both poor and high SiO_2/SiC qualities allowed establishing a theory based on the charge build-up mechanisms that take into account the complex oxide transition layer. Thus, this work represents an additional contribution to the research effort toward the fabrication of reliable (even in radiation environment) SiC MOS-based devices. The main results are summarized following two distinct parts:

Part A : Fabrication process optimization

1) After several attempts, an optimized gate oxide has been defined and developed using the rapid thermal process. This process involved a longer post-oxidation annealing under argon (chapter 5): The longer the annealing time, the better the self-arrangement of the crystal lattice after the oxidation and, consequently, the higher the oxide quality.

2) Phosphorus surface counter doping has been used to improve further the MOSFET gate oxide quality, increasing in this way the field effect mobility while maintaining an acceptable time stability of the threshold voltage (chapter 5) even at high temperatures (200ºC). However, this technique has shown two main drawbacks: The first one is that it generates some GIDL current that does not compromise the good device operation and that disappears with increasing temperature. The second one is that the measured V_{TH} is very close to 0V and, in some cases, tends to be negative (normally-on behavior). Thus, the surface counter doping dose still needs further optimization.

3) On-axis Al-implanted MOSFETs using the optimized gate oxide have shown very promising results at room temperature, much better than that of 8º Off axis Al-implanted MOSFETs. It should be mentioned the lack of mobility date of implanted MOSFETs in the literature. However, very high values of field effect mobility have been obtained in this work, not only peak values at low gate voltages but also at normal operating gate voltages. This is due to the high surface flatness leading to a lower roughness scattering effect. At high temperature and high gate voltage operation (V_{GS} > 12V), the field effect mobility of on-axis Al implanted MOSFETs is similar to that of 8º Off axis Al-implanted devices despite of a higher mobility peak observed at low gate voltages in the case of the on-axis MOSFETs. However, on-axis growth process could induce deep trap levels at the SiO_2/SiC interface that could avoid the accumulation process of MOS structures.

4) A curious V_{TH} variation at high temperatures has been observed (chapters 3,4,5 and 6) on all MOSFETs having an epitaxied p-body: It decreases with increasing temperature before starting to increase, and decreasing again. We suspected this variation to be connected to the existence of deep level defects within the 4H-SiC epilayer material. These deep levels only become active around 100ºC, and their effect start to disappear around 200ºC (temperature provides electrons enough energy for stepping to the conduction band).

Part B: Irradiation impact on 4H-SiC MOSFETs

1) Proton and electron irradiation processes on MOSFETs having a very poor oxide quality allowed, in some cases, correcting V_{TH} instabilities observed before the irradiation process and even increasing the field effect mobility. We suggested that irradiation not only generates a negative impact on the MOSFETs like deep defect creation or e-h pair's generation within the structure, but also it might induce a small diffusion of some passivating species. Concretely, diffusion of nitrogen or hydrogen (in a minor extend) located at the SiO_2/SiC interface could predominate over the other mentioned negative effects, contributing to enhance the SiO_2/SiC interface quality (chapters 3 and 6). However, the improvement of the observed electrical parameters depends on the irradiation dose, energy, and also on the gate oxide quality. It seemed that irradiated MOSFETs at low energies (0.18 MeV) are less robust as the fluence increases, contrarily to what happens at high irradiation energies. This is a consequence of a huge amount of damage at the epilayer surface at low irradiation energies. Nevertheless, the irradiation process did generally not increase either the gate leakage currents or the oxide breakdown voltage.

2) Due to the observed V_{TH} variation of the irradiated MOSFET, this study has put in evidence the existence of a threshold irradiation fluence that changed the interface trap predominance at the SiO_2/SiC interface from donor to acceptor (chapters 3 and 6).

3) A complete recovery of electrical parameters induced by the post-irradiation annealing process is very rare (chapters 3 and 4) and, when it occurs, is only partial in most of the studied cases. This is because a true annealing is very difficult to obtain. Indeed, contrary to Si MOSFETs, interface charge traps play an important role. We suspect that during the post-irradiation annealing not only E´ centers can be partially fulfilled, but other phenomena can also be considered:

- Extra nitrogen diffusion.
- Charge tunneling of ion charges generated by irradiation in the epitaxial layer at the vicinity of the SiO_xN_y transition layer, that can recombine inside the transition layer or be trapped by the interface traps.
- Trapping of e-h pairs within the oxide.

- Hydrogen atom formation inside the p-body.

Among them, the most predominant phenomenon will determine the electrical parameter behavior after the post-irradiation annealing process. However, in most of the cases, it seemed that the predominant scattering mechanism at both high temperature annealing and high gate voltages (>12V) is the roughness scattering.

4) Proton irradiation performed on MOSFETs having a good SiO_2/SiC interface quality has shown a decrease of GIDL current (chapter 6) with the fluence increase. In general, the irradiation robustness limit for nMOSFETs having an oxynitrided gate oxide is reached at a fluence of $5 \cdot 10^{13}$ cm^{-2} for all energies.

ANNEX

A1) Irradiation Data of 0.18 MeV of MOSFET (1)

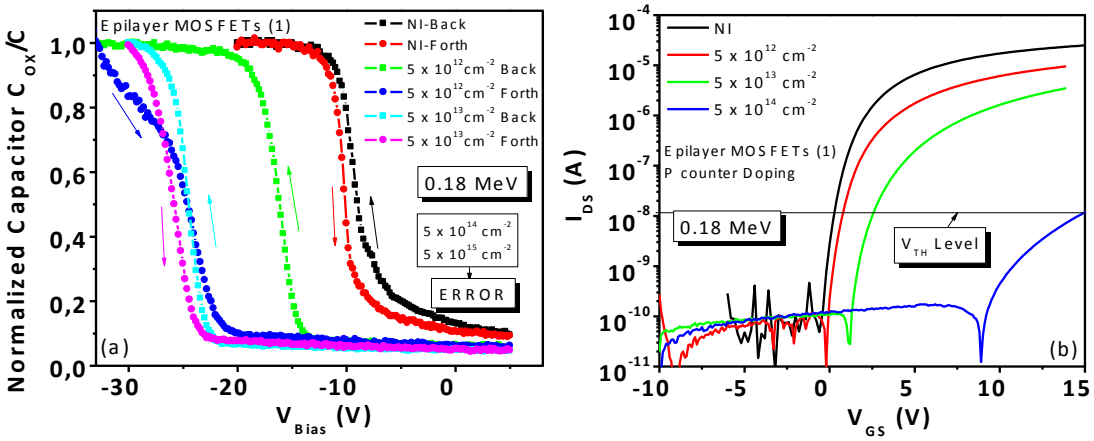


Fig A.6.1. Normalized capacitance, hysteresis variation (a) and transconductance characteristics (b) of non-irradiated and irradiated MOSFET (1) at 0.18 MeV following different fluences ($5 \cdot 10^{12}$ cm^{-2}, $5 \cdot 10^{13}$ cm^{-2}, $5 \cdot 10^{14}$ cm^{-2}). All MOSFET (1) contain an aluminum epilayer well and phosphorus surface counter doping and his epilayer substrate is oriented 8ºoff-axis.

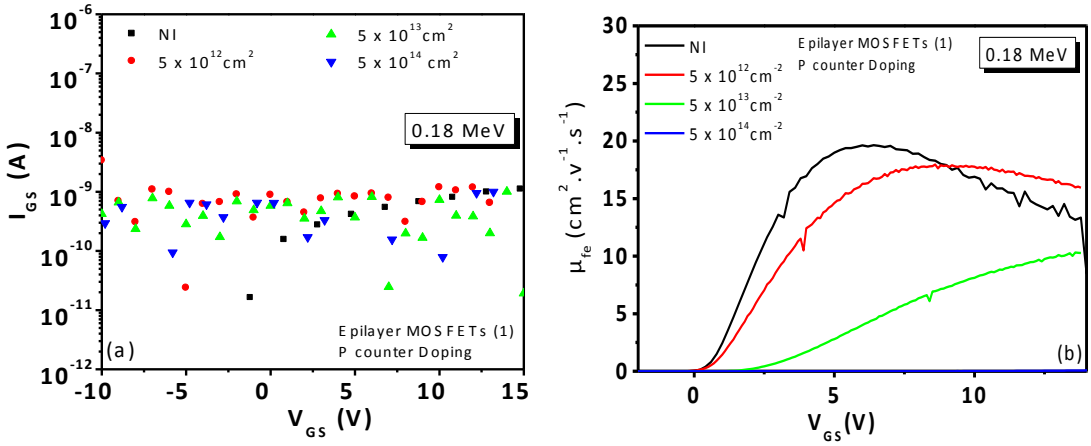


Fig A.6.2. $I_{GS}(V_{GS})$ characteristics (a) and $\mu_{fe}(V_{GS})$ (b) of non-irradiated and irradiated MOSFET (1) at 0.18 MeV following different fluences.

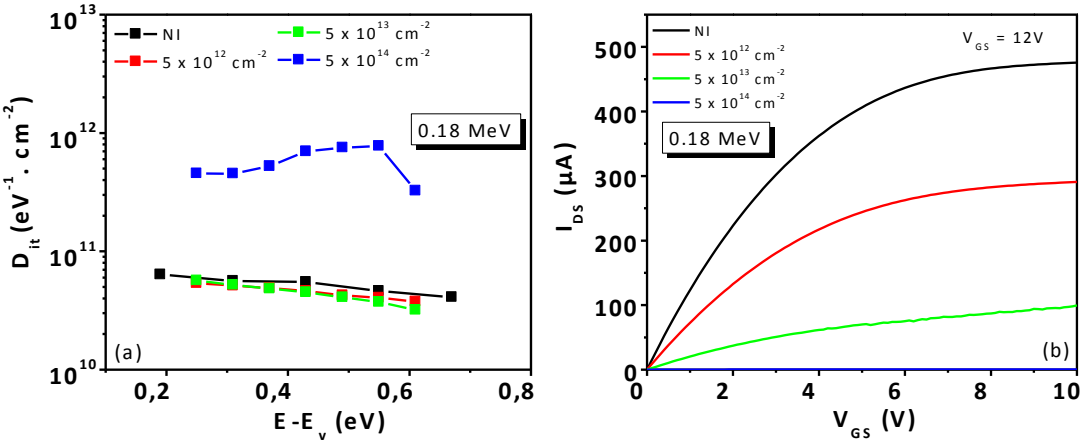


Fig A.6.3. D_{it} variation above the valence band (a) and I_{DS} (V_{DS}) (b) of non-irradiated and irradiated MOSFET (1) at 0.18 MeV following different fluences.

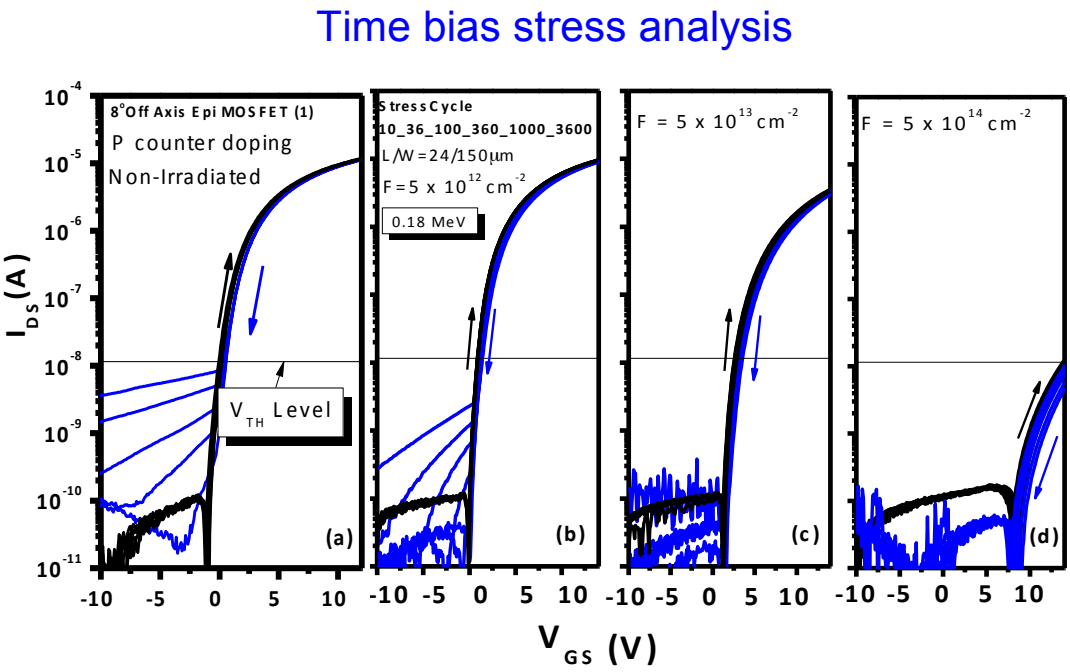


Fig A.6.4. BSI Transconductance characteristic of MOSFET (1) non-irradiated (a) and irradiated at 0.18 MeV with $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c) and $5{\cdot}10^{14}$ cm^{-2} (d) proton fluence.

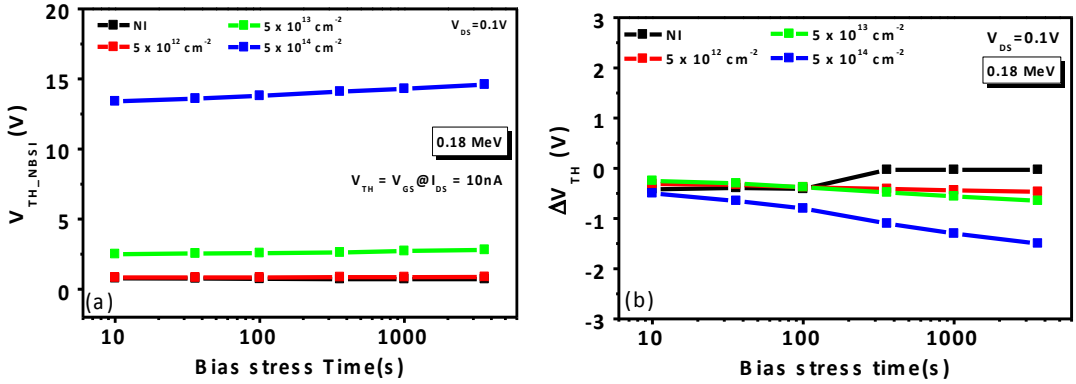


Fig A.6.5. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFET (1) irradiated at 0.18 MeV.

A2) Post irradiation annealing, data of 0.18 MeV of MOSFET (1)

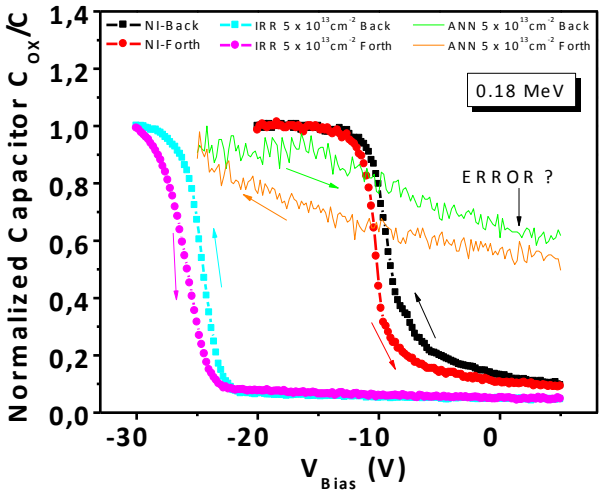


Fig A.6.6. Normalized capacitance, hysteresis variation of non-irradiated, irradiated and post irradiation annealing MOSFET (1) irradiated at 0.18 MeV with a fluence of $5 \cdot 10^{13}$ cm^{-2}.

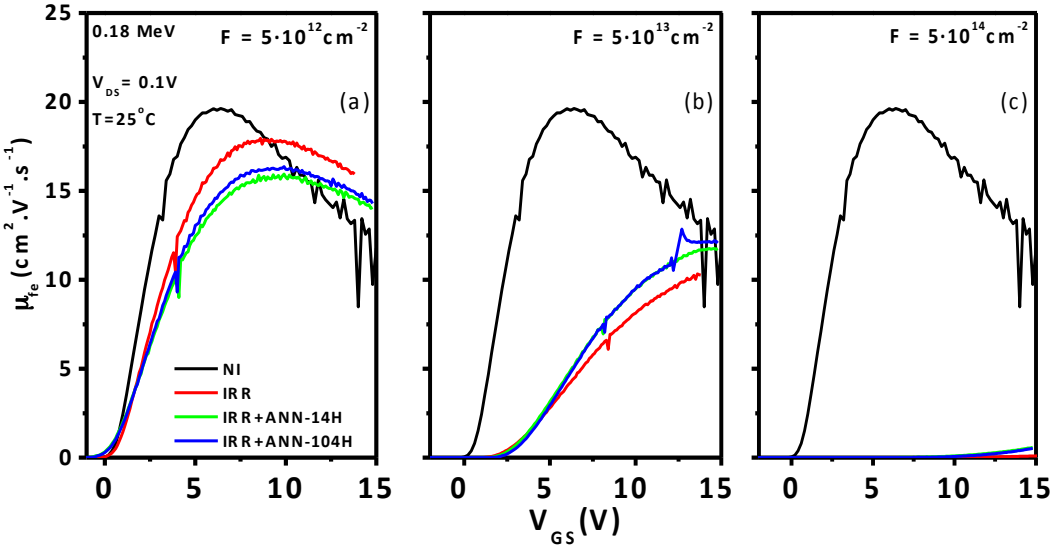


Fig A.6.7. The field effect mobility time evolution for 0.18 MeV proton irradiated MOSFET (1) at $5 \cdot 10^{12} cm^{-2}$ (a), $5 \cdot 10^{13} cm^{-2}$ (b) and $5 \cdot 10^{14} cm^{-2}$ (c) after irradiation and post irradiation annealing time (14h, 104h).

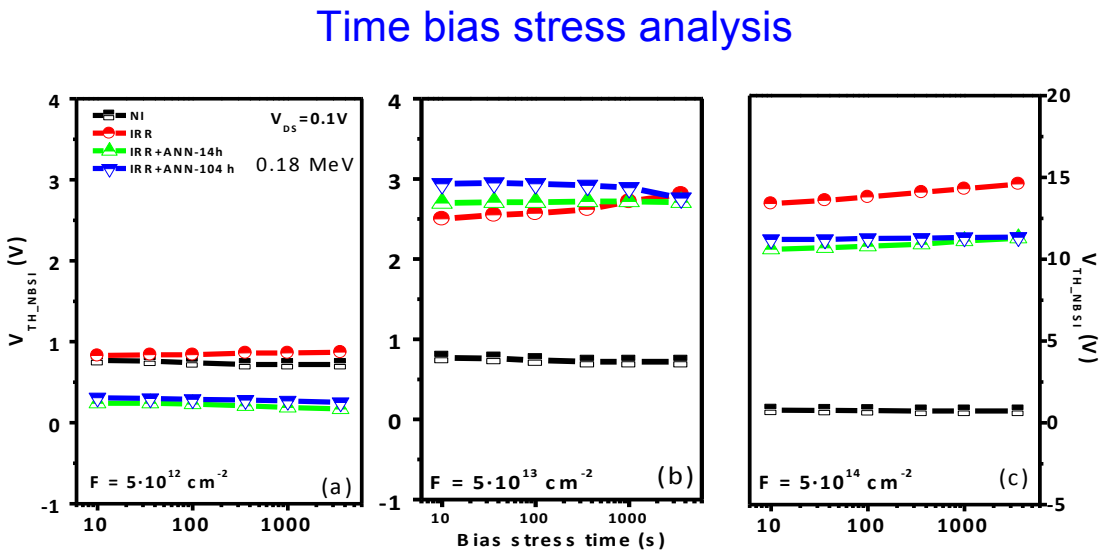


Fig A.6.8. The threshold voltage time evolution after a negative bias stress for 0.18 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

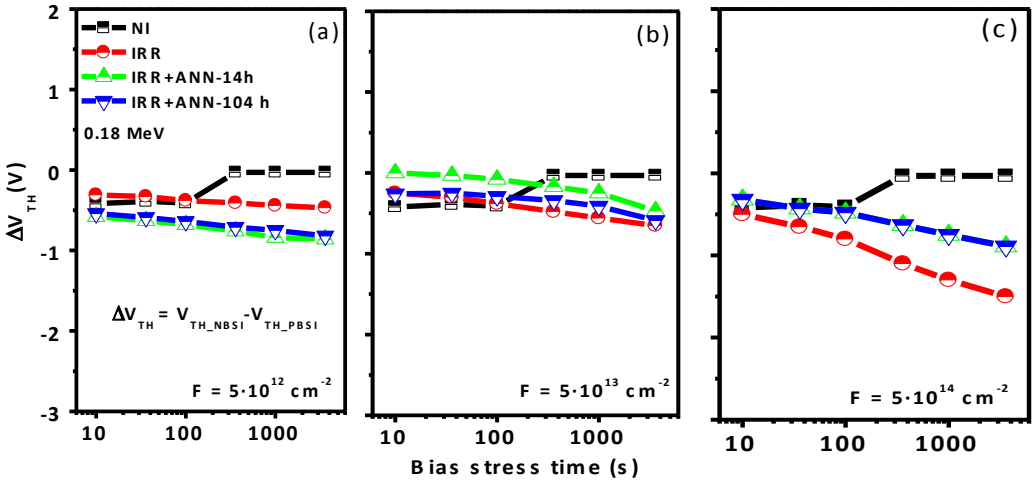


Fig A.6.9. The threshold voltage hysteresis time evolution after a 0.18 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

A3) Post irradiation annealing: Temperature analysis data of 0.18 MeV of MOSFET (1)

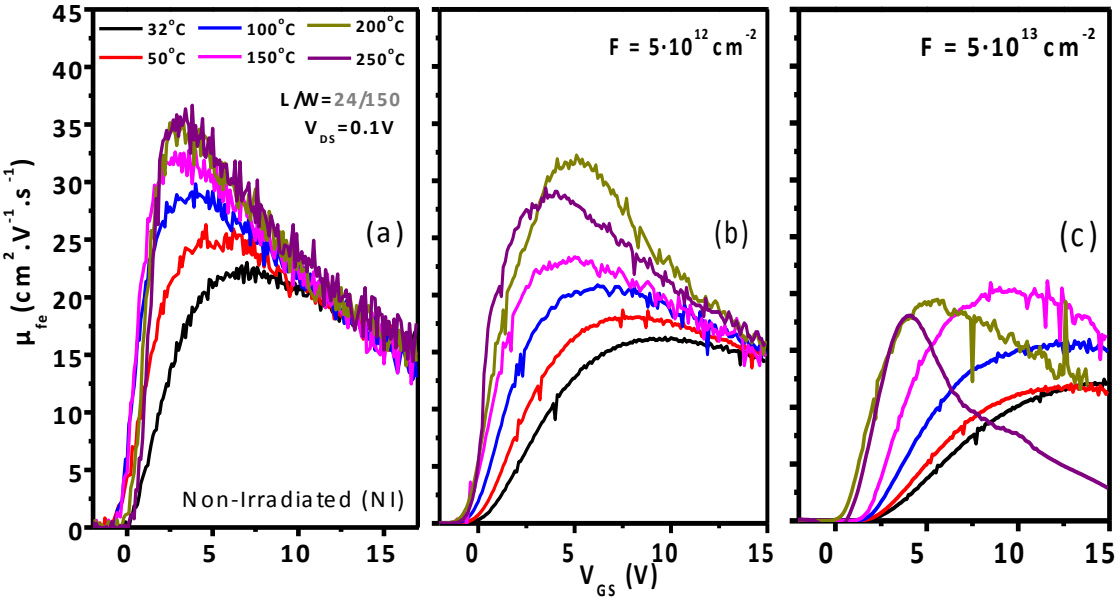


Fig. A.6.10. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFET irradiated at 0.18 MeV with a proton dose of $5{\cdot}10^{12}$ cm^{-2} (b) and $5{\cdot}10^{13}$ cm^{-2} (c).

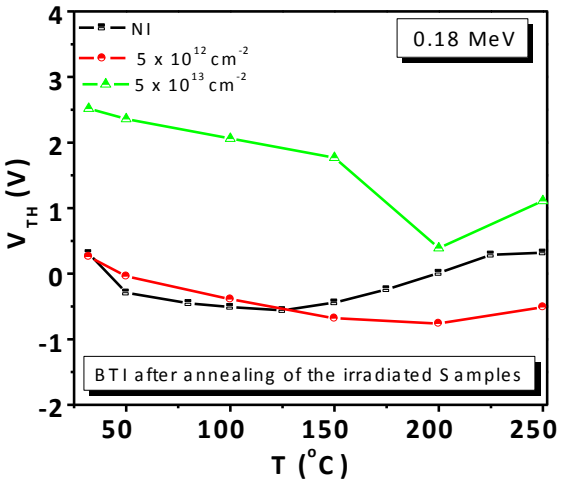


Fig A.6.11. The V_{TH} temperature evolution for the NI MOSFET and post irradiation annealed MOSFET (1) of all fluences and doses at a proton irradiation of 0.18 MeV.

A4) Irradiation Data of 10 MeV of MOSFET (1)

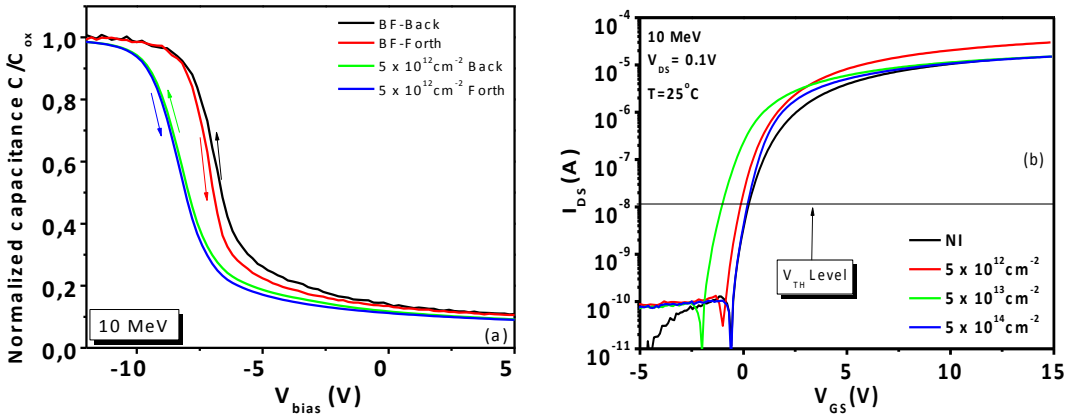


Fig A.6.12. Normalized capacitance (a) and transconductance characteristics (b) of non-irradiated and irradiated MOSFET (1) at 10 MeV following different fluences ($5{\cdot}10^{12}$ cm^{-2}, $5{\cdot}10^{13}$ cm^{-2}, $5{\cdot}10^{14}$ cm^{-2}).

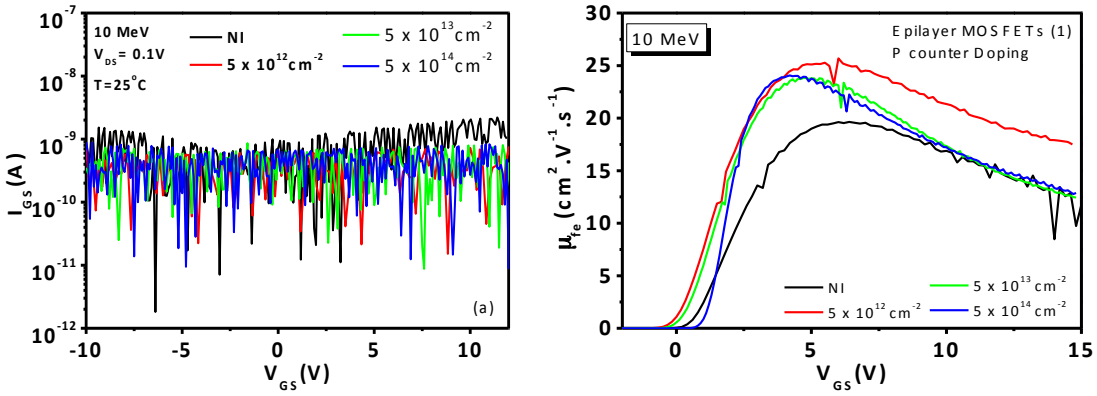


Fig A.6.13. $I_{GS}(V_{GS})$ characteristics (a) and $\mu_{fe}(V_{GS})$ (b) of non-irradiated and irradiated MOSFET (1) at 10 MeV following different fluences.

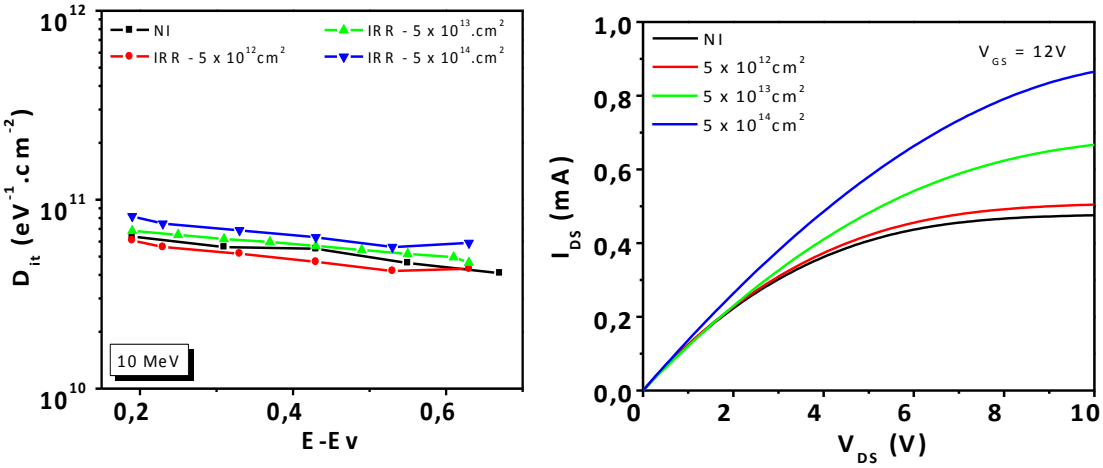


Fig A.6.14. D_{it} variation above the valence band (a) and $I_{DS}(V_{DS})$ (b) of non-irradiated and irradiated MOSFET (1) at 10 MeV following different fluences.

Time bias stress analysis

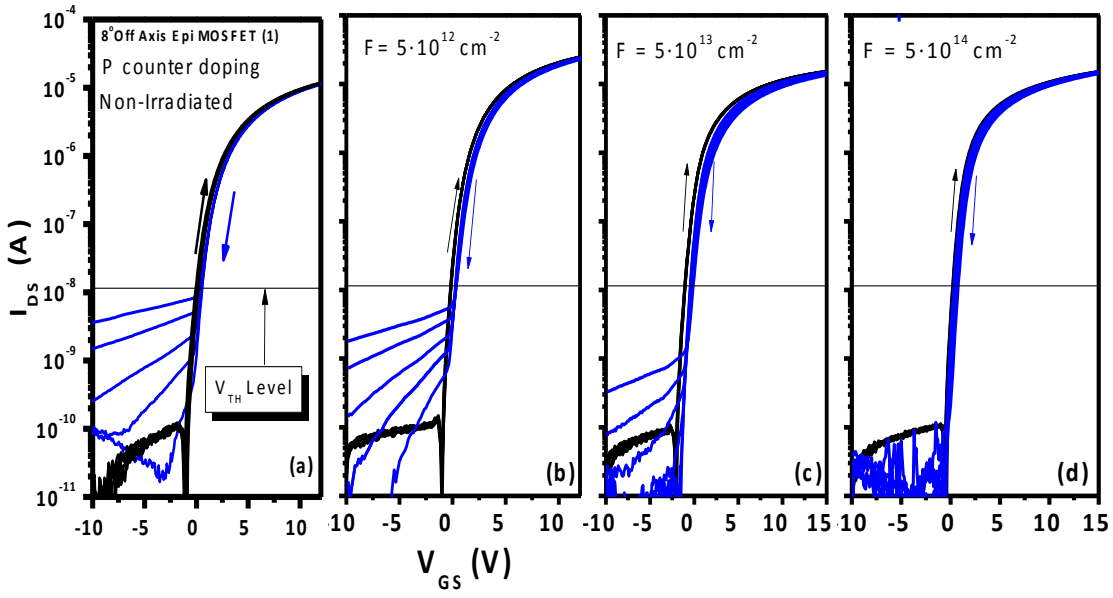


Fig A.6.15. BSI Transconductance characteristic of MOSFET (1) non-irradiated (a) and irradiated at $5 \cdot 10^{12}$ cm^{-2} (b), $5 \cdot 10^{13}$ cm^{-2} (c), $5 \cdot 10^{14}$ cm^{-2} (d) with a 10MeV proton beam.

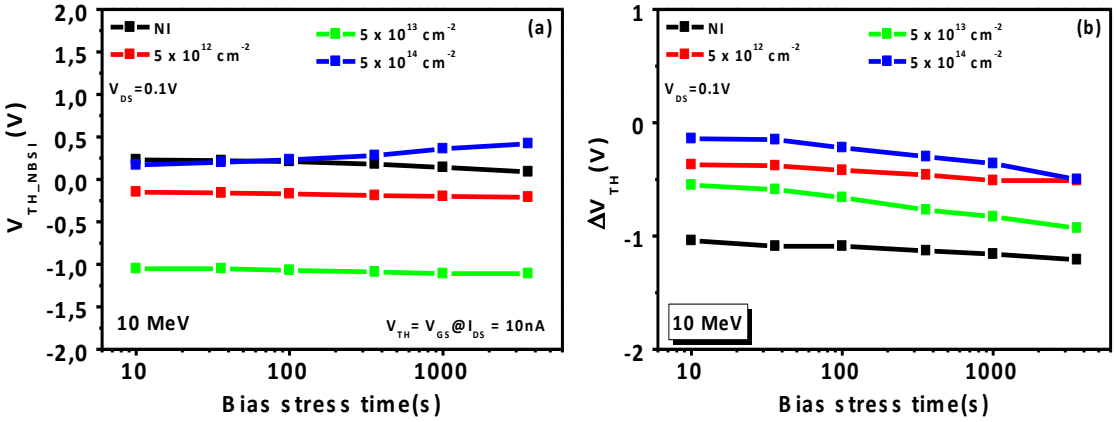


Fig A.6.16. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFET (1) irradiated at 10 MeV.

A5) Post irradiation annealing, temperature analysis data of 10 MeV of MOSFET (1)

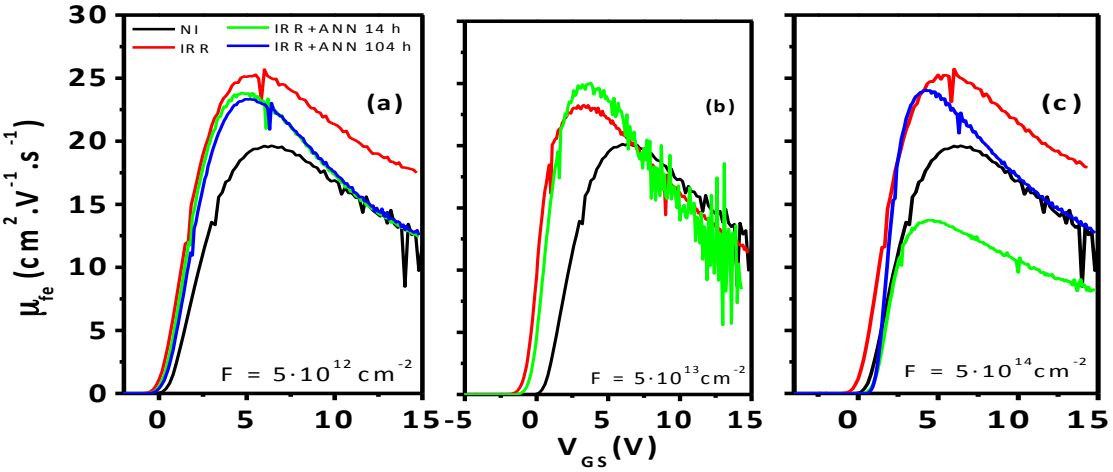


Fig A.6.17. The field effect mobility time evolution for 10 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$$cm^{-2}$ (b) and $5{\cdot}10^{14}$$cm^{-2}$ (c) after irradiation and several post irradiation annealing time (14h, 104h).

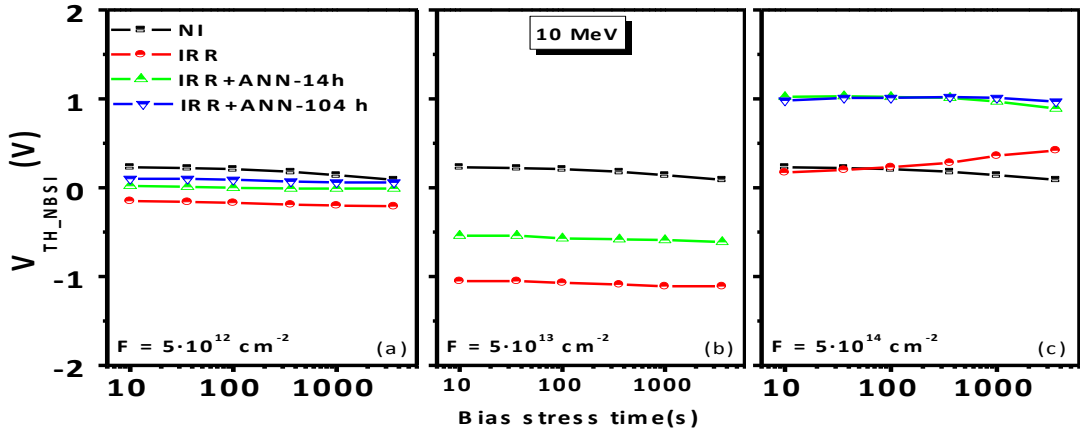


Fig A.6.18. The threshold voltage time evolution after a negative bias stress for 10 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

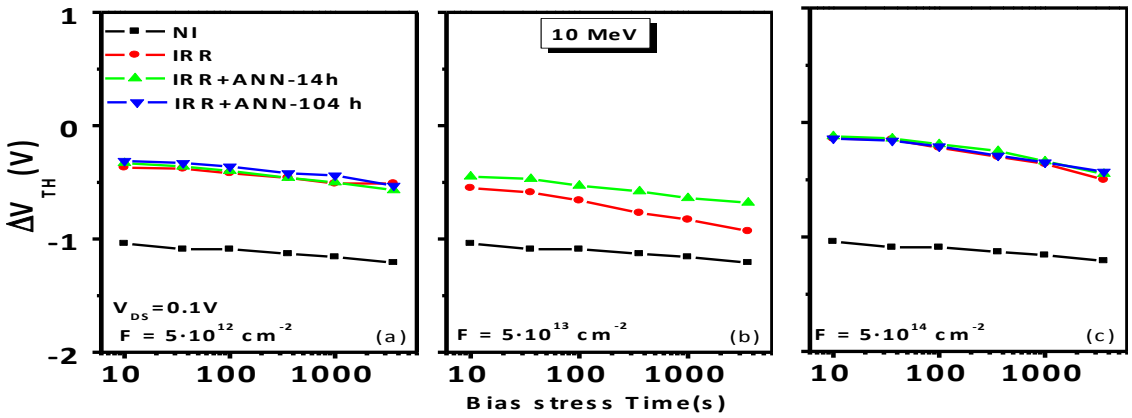


Fig A.6.19. The threshold voltage hysteresis time evolution after a 10 MeV proton irradiated MOSFET (1) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

A6) Post irradiation annealing, temperature analysis data of 10 MeV of MOSFET (1)

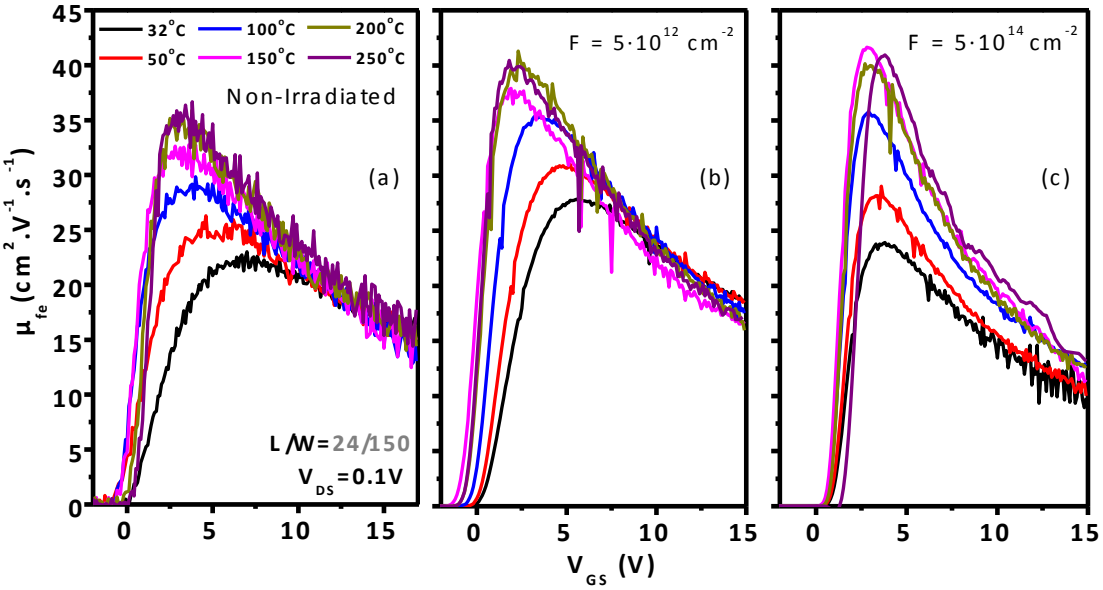


Fig. A.6.20. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFET irradiated at 10 MeV with a proton dose of $5 \cdot 10^{12}$ cm^{-2} (b) and $5 \cdot 10^{13}$ cm^{-2} (c).

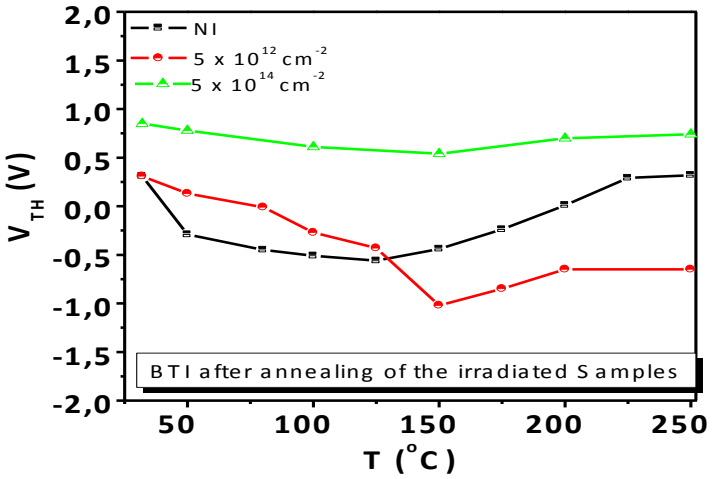


Fig A.6.21. The V_{TH} temperature evolution for the NI MOSFET and post irradiation annealed MOSFET (1) of all fluences and doses at a proton irradiation of 10 MeV.

B1) Irradiation Data of 0.18 MeV of MOSFET (2)

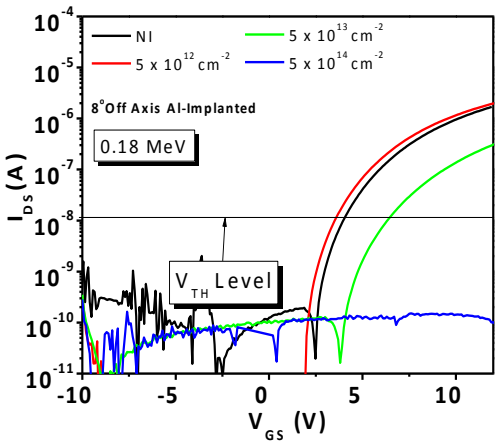


Fig B.6.22. Transconductance characteristics of non-irradiated and irradiated MOSFET (2) at 0.18 MeV following different fluences ($5{\cdot}10^{12}$ cm^{-2}, $5{\cdot}10^{13}$ cm^{-2}, $5{\cdot}10^{14}$ cm^{-2}). All MOSFET (2) contain an aluminum implanted well and its epilayer substrate is oriented 8ºoff-axis.

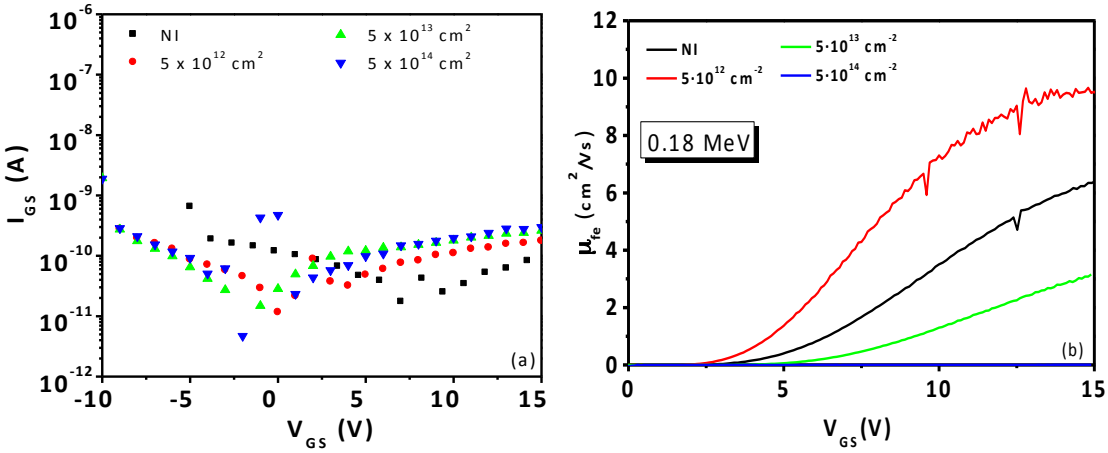


Fig B.6.23. $I_{GS}(V_{GS})$ characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFET (2) at 0.18 MeV following different fluences.

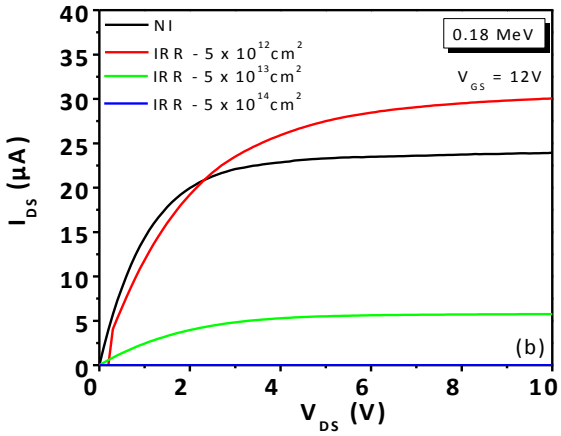


Fig B.6.24. I_{DS} (V_{DS}) of non-irradiated and irradiated MOSFET (2) at 0.18 MeV following different fluences.

Time bias stress analysis

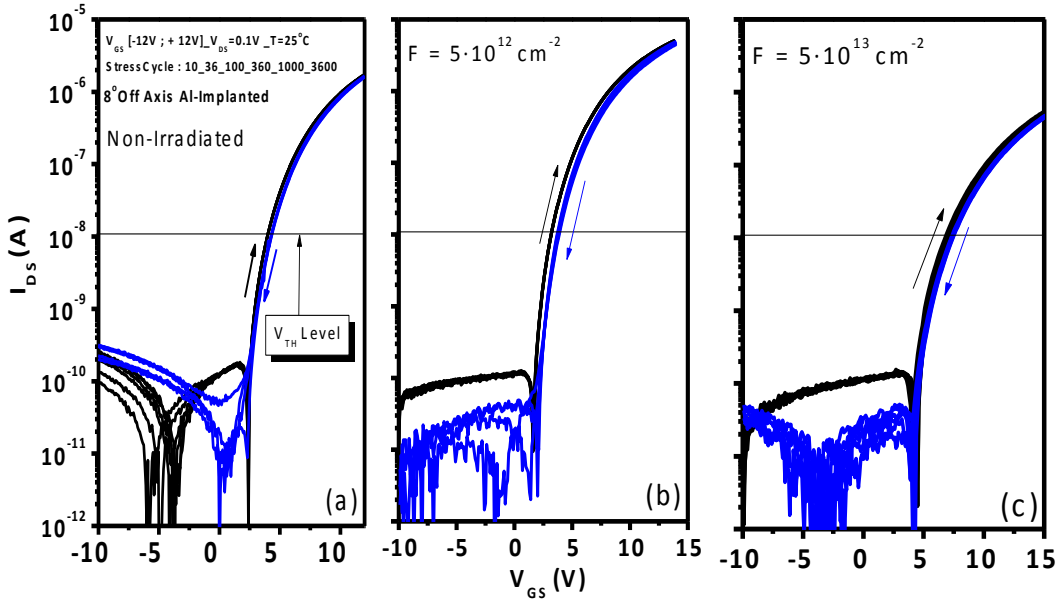


Fig B.6.25. Transconductance characteristic of MOSFET (2) non-irradiated (a) and irradiated at 0.18 MeV and at $5 \cdot 10^{12}$ cm^{-2} (b), $5 \cdot 10^{13}$ cm^{-2} (c) proton fluence.

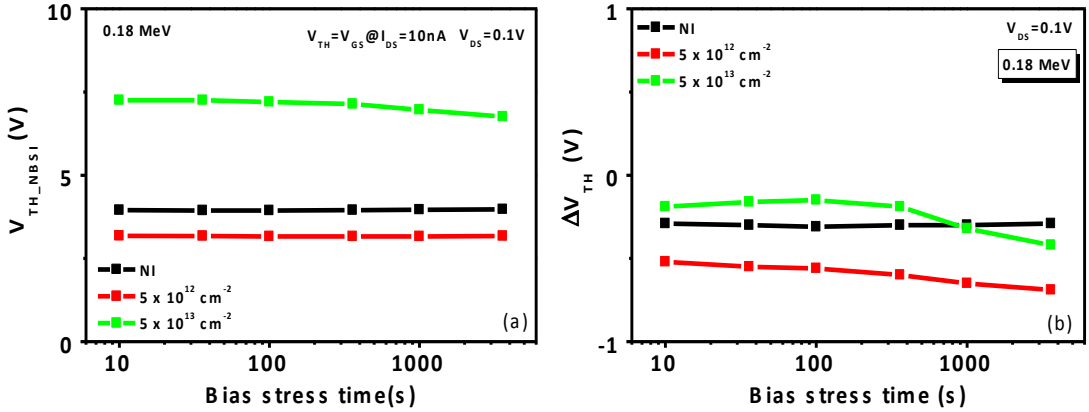


Fig B.6.26. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFET (2) irradiated at 0.18 MeV.

B2) Post irradiation annealing, temperature analysis data of 0.18 MeV of MOSFET (2)

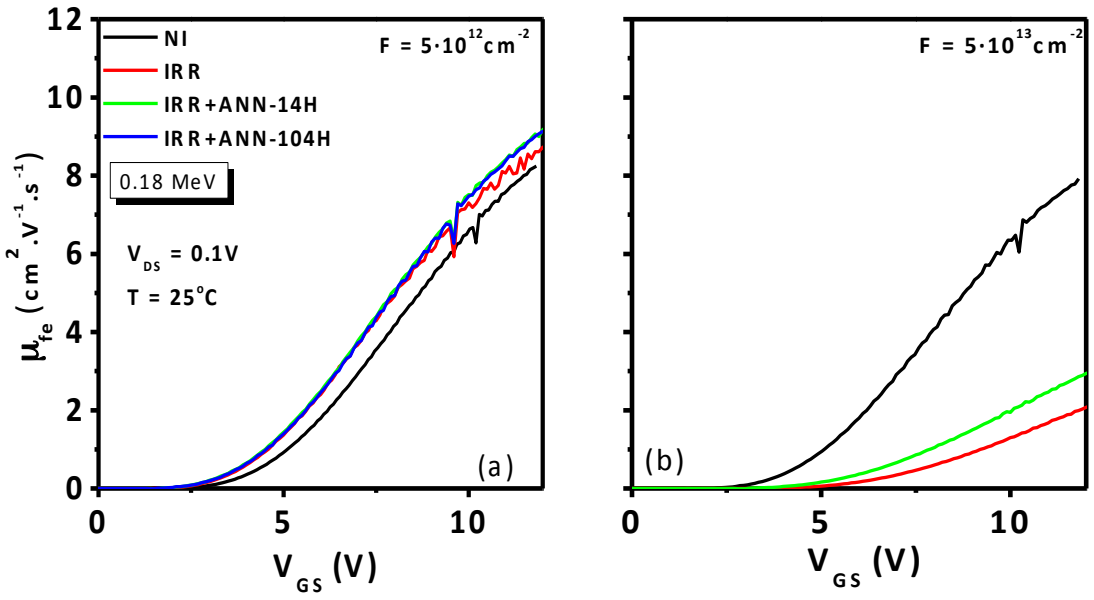


Fig B.6.27. The field effect mobility time evolution for 0.18 MeV proton irradiated MOSFET (2) at $5 \cdot 10^{12}$ cm^{-2} (a), $5 \cdot 10^{13} cm^{-2}$ (b) after irradiation and several time annealing (14h, 104h).

Time bias stress analysis

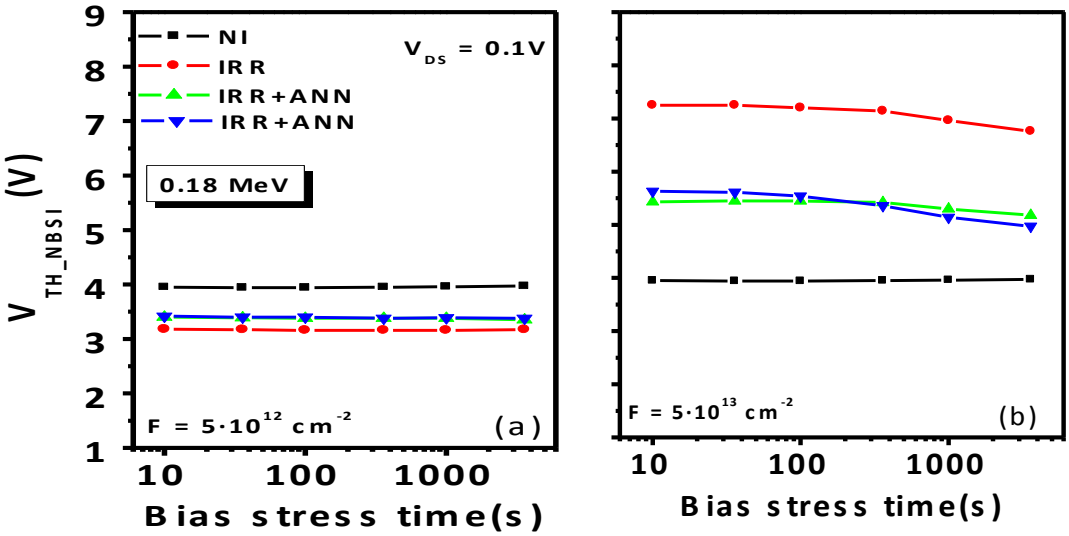


Fig B.6.28. The threshold voltage time evolution after a negative bias stress for 0.18 MeV proton irradiated MOSFET (2) at $5 \cdot 10^{12}$ cm^{-2} (a), $5 \cdot 10^{13}$ cm^{-2} (b) after irradiation and several post irradiation annealing time (14h, 104h).

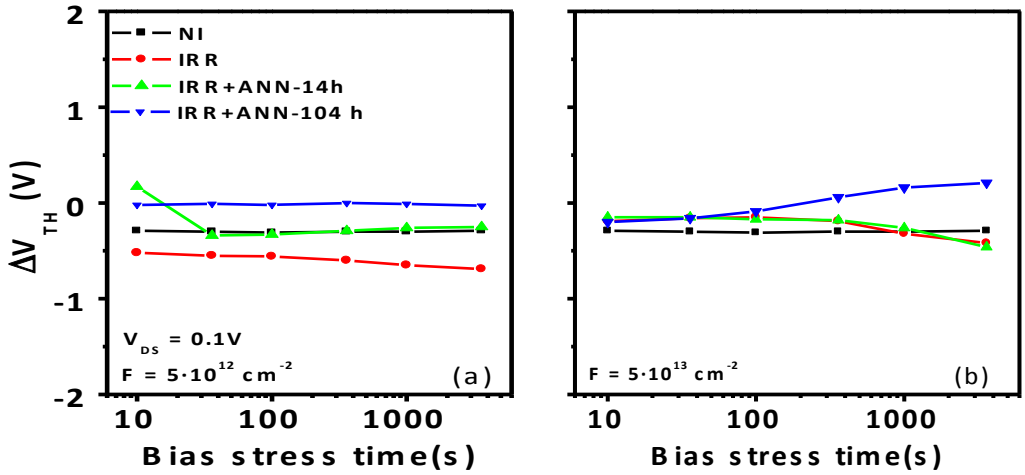


Fig B.6.29. The threshold voltage hysteresis time evolution after a 0.18 MeV proton irradiated MOSFET (2) at $5 \cdot 10^{12}$ cm^{-2} (a), $5 \cdot 10^{13}$ cm^{-2} (b) after irradiation and several post irradiation annealing time (14h, 104h).

B3) Post irradiation annealing, temperature analysis data of 0.18 MeV of MOSFET (2)

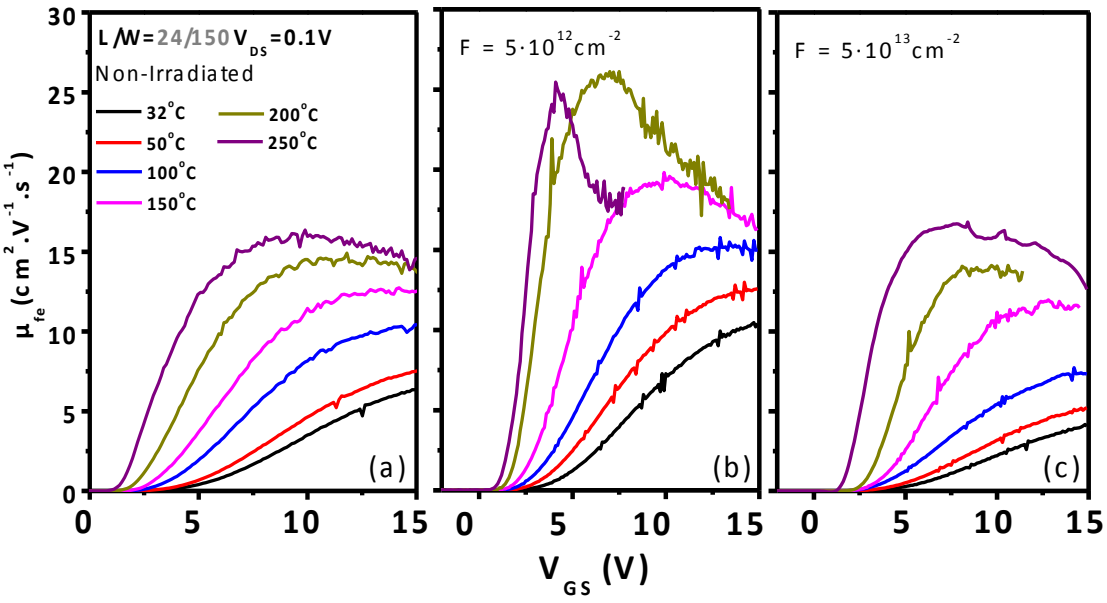


Fig. B.6.30. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFET (2) irradiated at 0.18 MeV with a proton dose of $5 \cdot 10^{12}$ cm^{-2} (b) and $5 \cdot 10^{13}$ cm^{-2} (c).

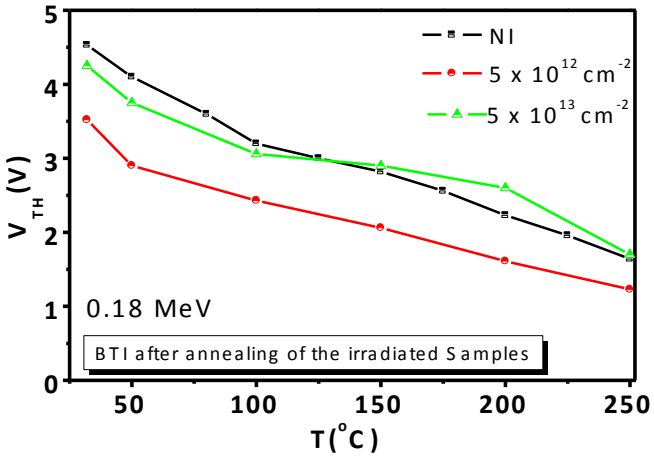


Fig B. 6.31. The V_{TH} temperature evolution for the NI MOSFET and post irradiation annealed MOSFET (2) of all fluences and doses at a proton irradiation of 0.18 MeV.

B4) Irradiation Data of 10 MeV of MOSFET (2)

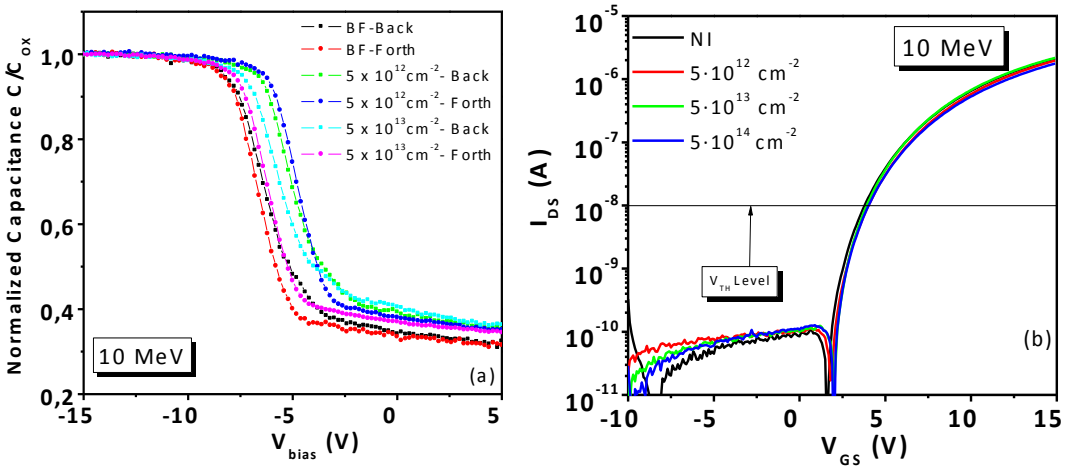


Fig B.6.32. Normalized capacitance, hysteresis capacitance (a) and transconductance characteristics (b) of non-irradiated and irradiated MOSFET (2) at 10 MeV following different fluences.

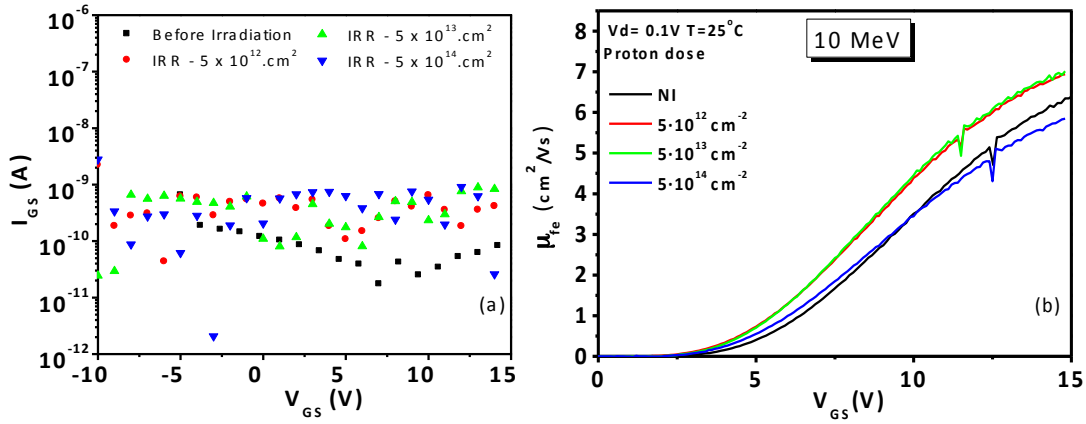


Fig B.6.33. $I_{GS}(V_{GS})$ characteristics (a) and μ_{fe} (V_{GS}) (b) of non-irradiated and irradiated MOSFETs (2) at 10 MeV following different fluences.

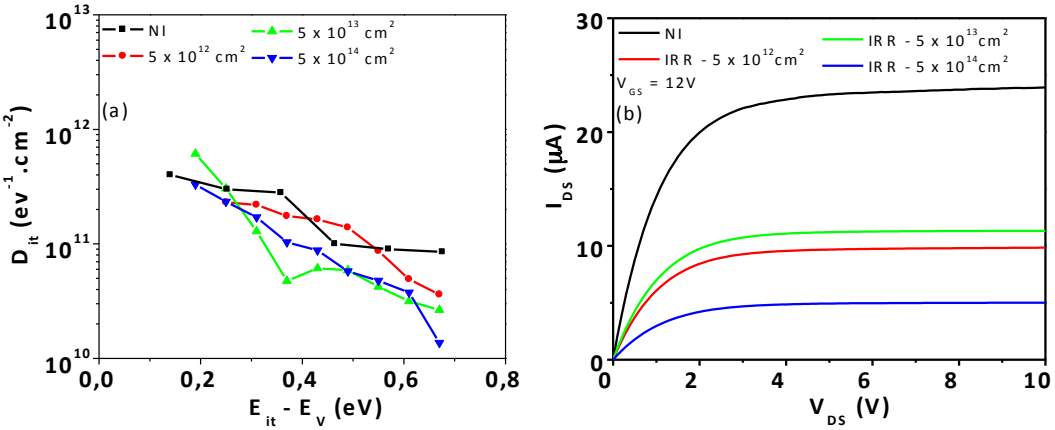


Fig B.6.34. D_{it} variation above the valence band (a) and I_{DS} (V_{DS}) (b) of non-irradiated and irradiated MOSFETs (2) at 10 MeV following different fluences.

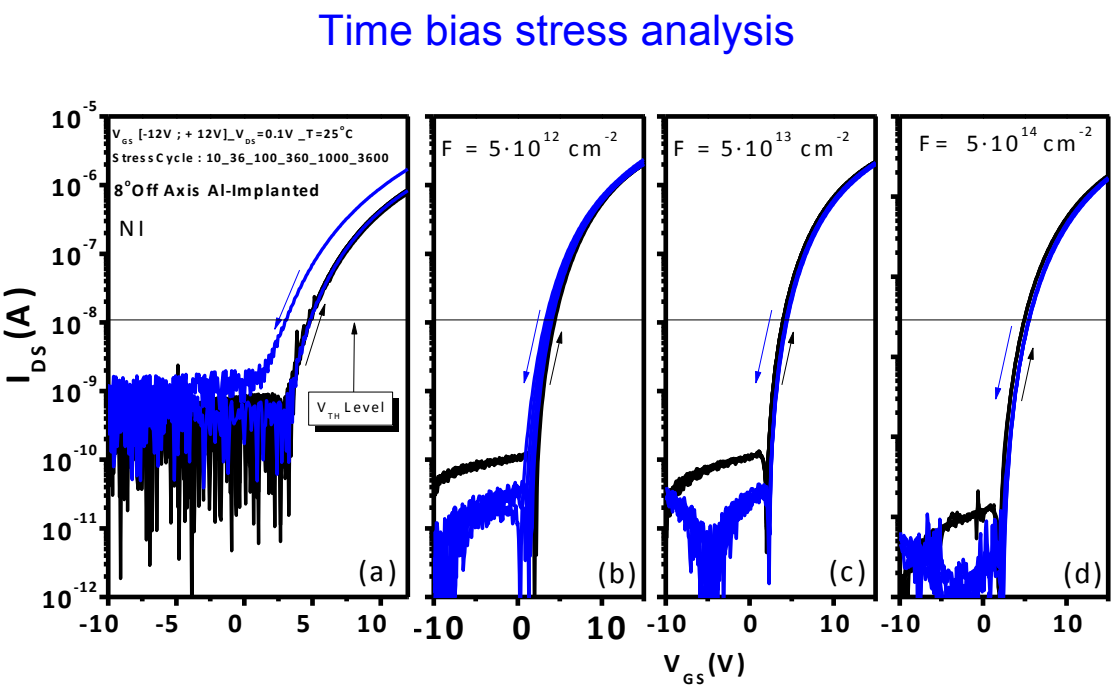


Fig B.6.35. BSI Transconductance characteristic of MOSFETs (2) non-irradiated (a) and irradiated at $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c), $5{\cdot}10^{14}$ cm^{-2} (d) under 10 MeV proton beam.

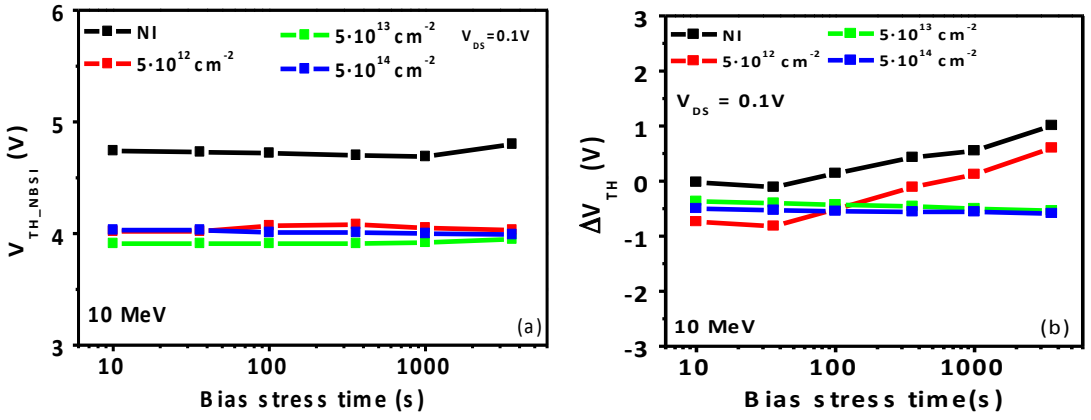


Fig B.6.36. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFETs (2) irradiated at 10 MeV.

B5) Post irradiation annealing, temperature analysis data of 10 MeV of MOSFET (2)

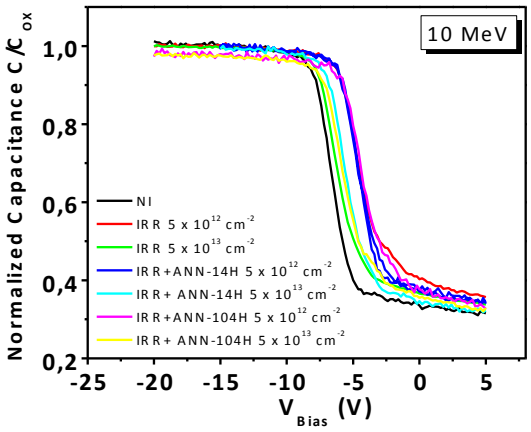


Fig B.6.37. Normalized capacitance, hysteresis variation of non-irradiated, irradiated and post irradiation annealing MOSFET (2) irradiated at 10 MeV with a fluence of $5 \cdot 10^{12}$ cm^{-2}.

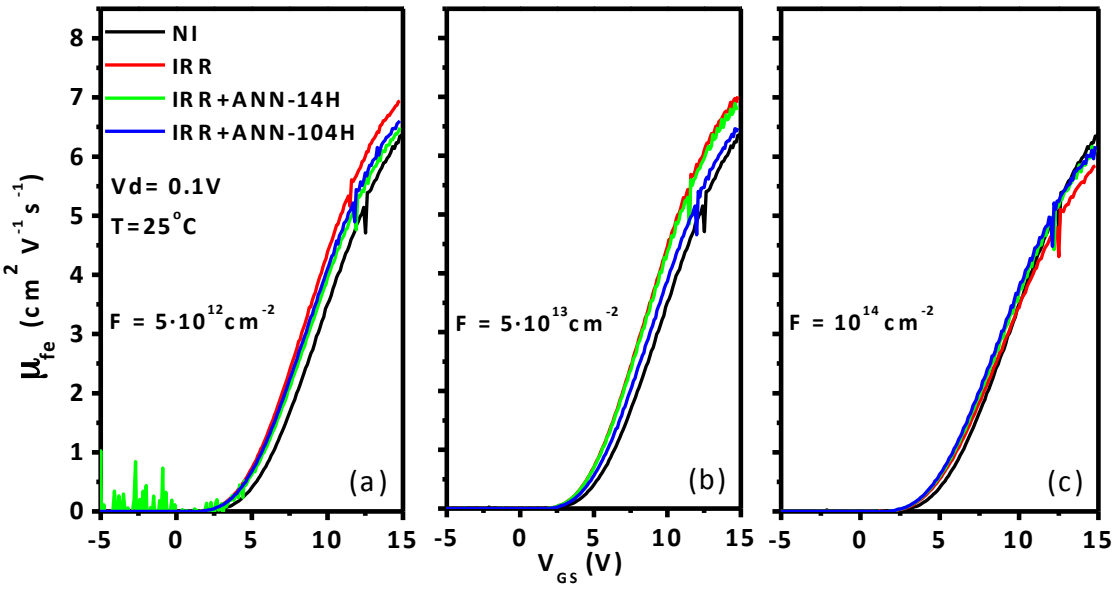


Fig B.6.38. The field effect mobility time evolution for 10 MeV proton irradiated MOSFET (1) at $5 \cdot 10^{12} cm^{-2}$ (a), $5 \cdot 10^{13} cm^{-2}$ (b) and $5 \cdot 10^{14} cm^{-2}$ (c) after irradiation and post irradiation annealing time (14h, 104h).

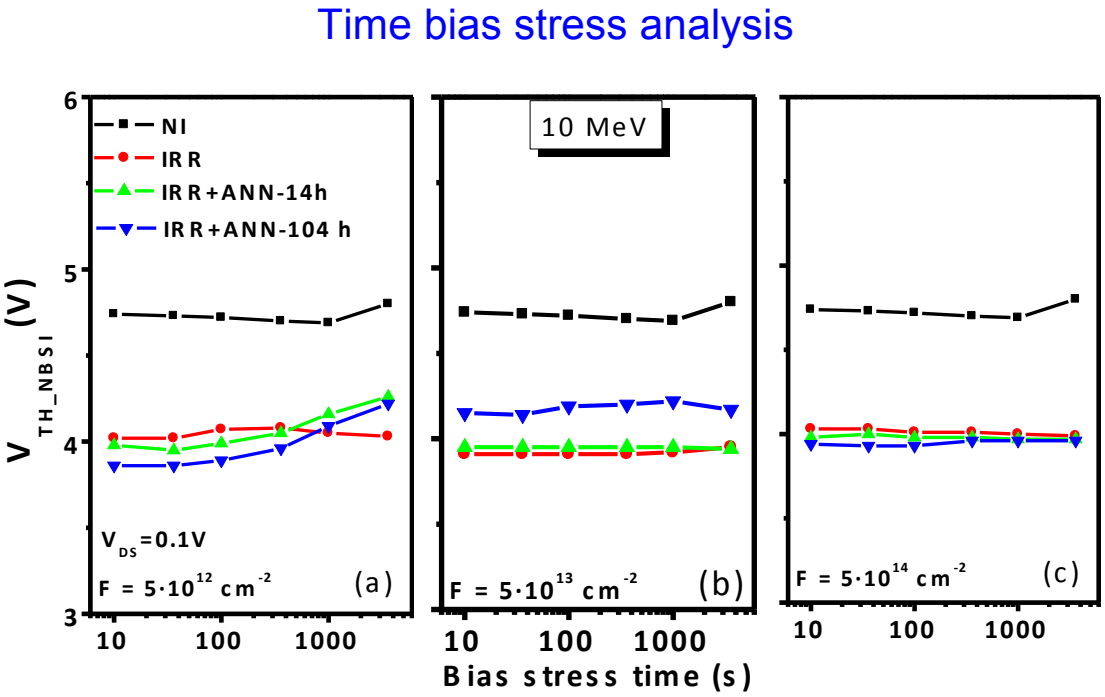


Fig B.6.39. The threshold voltage time evolution after a negative bias stress for 10 MeV proton irradiated MOSFETS (2) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

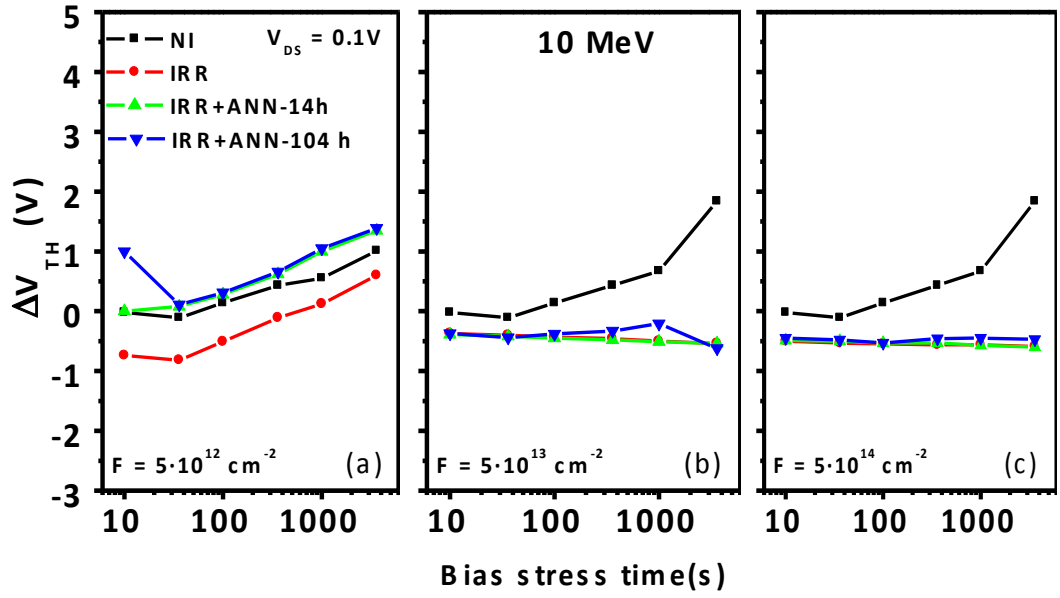


Fig B.6.40. The threshold voltage hysteresis time evolution after a 10 MeV proton irradiated MOSFETS (2) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

B6) Post irradiation annealing, temperature analysis data of 10 MeV of MOSFET (2)

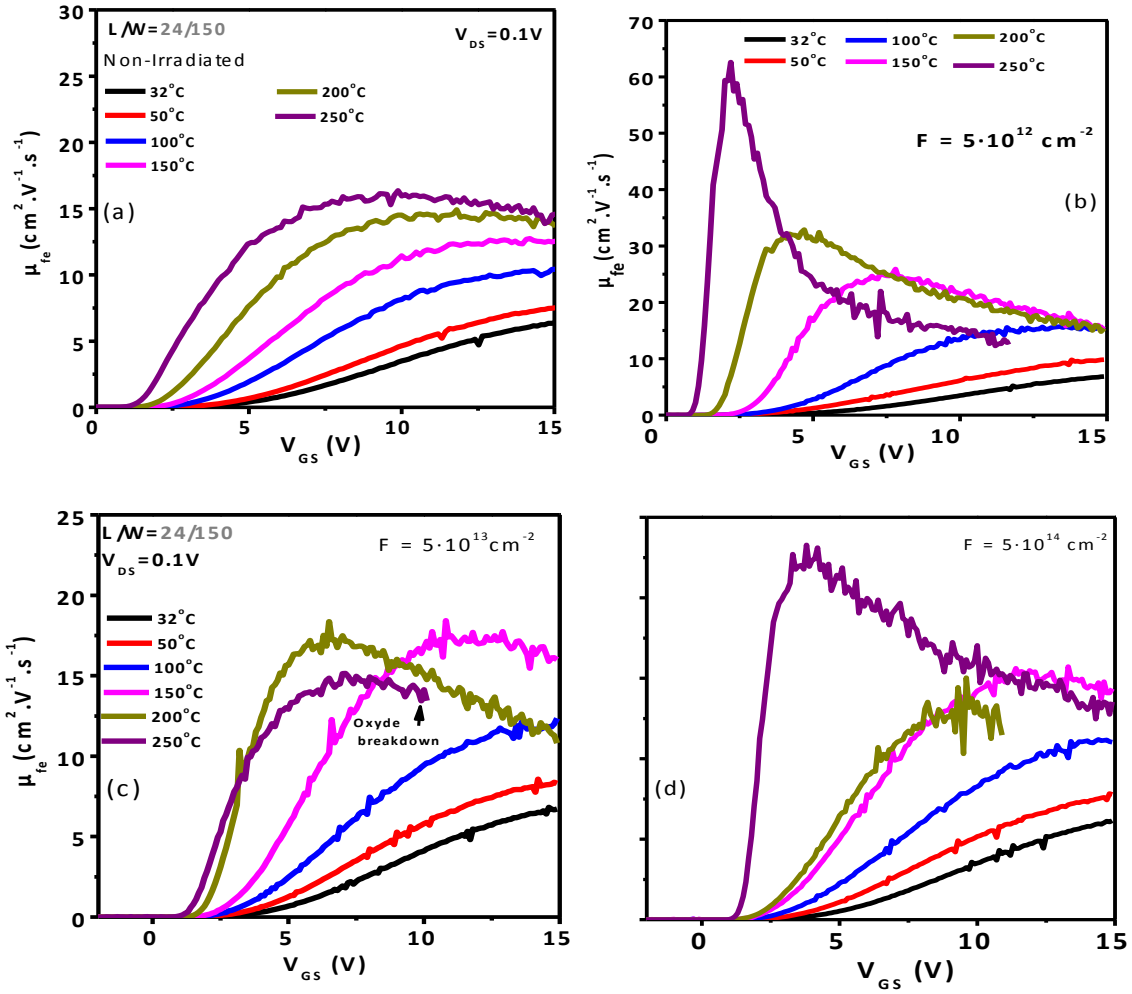


Fig. B.6.41. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFETs irradiated at 10 MeV with a proton dose of $5 \cdot 10^{12}$ cm^{-2} (b), $5 \cdot 10^{13}$ cm^{-2} (c) and $5 \cdot 10^{13}$ cm^{-2} (d).

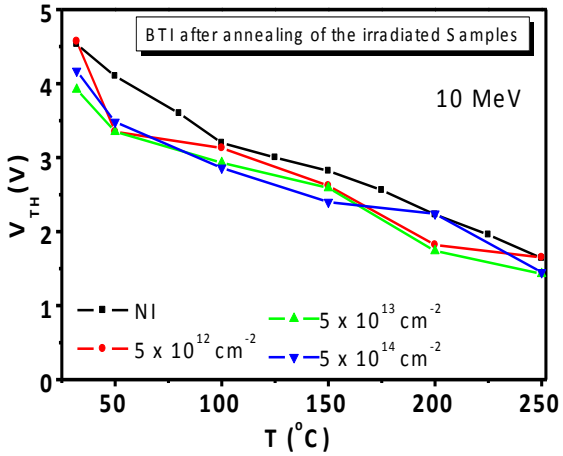


Fig B.6.42. The V_{TH} temperature evolution for the NI MOSFETs and post irradiation annealed MOSFETs (2) of all fluences and doses at a proton irradiation of 10 MeV.

C1) Irradiation Data of 0.18 MeV of MOSFET (3)

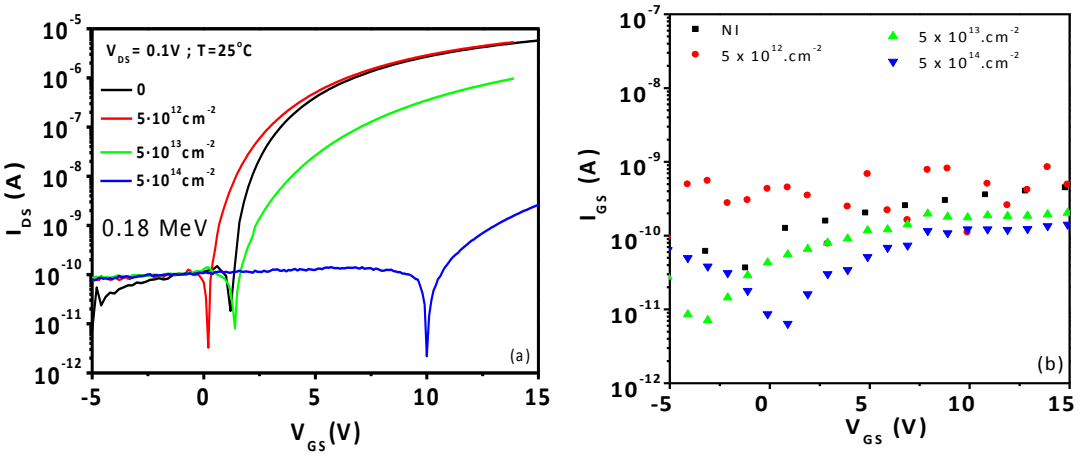


Fig C.6.43. Transconductance characteristics (a) and $I_{GS}(V_{GS})$ characteristics (b) of non-irradiated and irradiated MOSFET (3) at 0.18 MeV following different fluences ($5{\cdot}10^{12}$ cm^{-2}, $5{\cdot}10^{13}$ cm^{-2}, $5{\cdot}10^{14}$ cm^{-2}). All MOSFETs (3) contain an aluminum implanted well and its epilayer substrate is oriented on-axis.

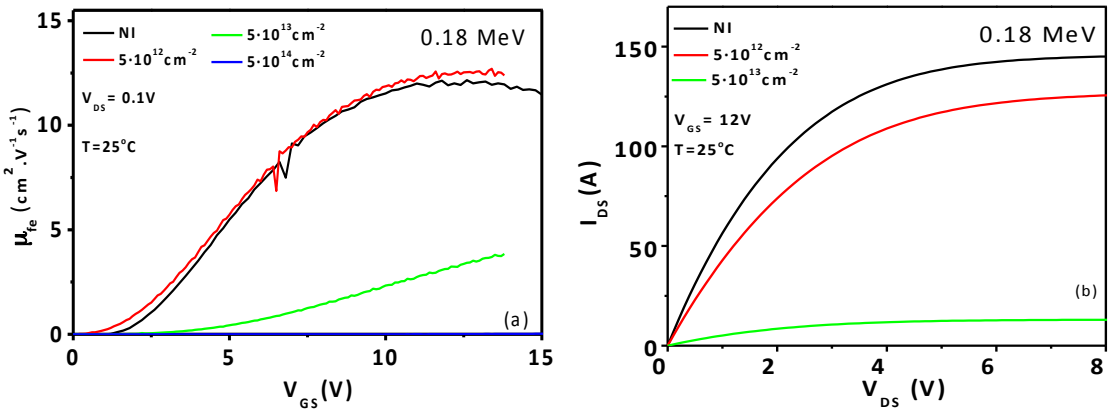


Fig C.6.44. μ_{fe} (V_{GS}) (a) and I_{DS} (V_{DS}) (b) of non-irradiated and irradiated MOSFETs (3) at 0.18 MeV following different fluences.

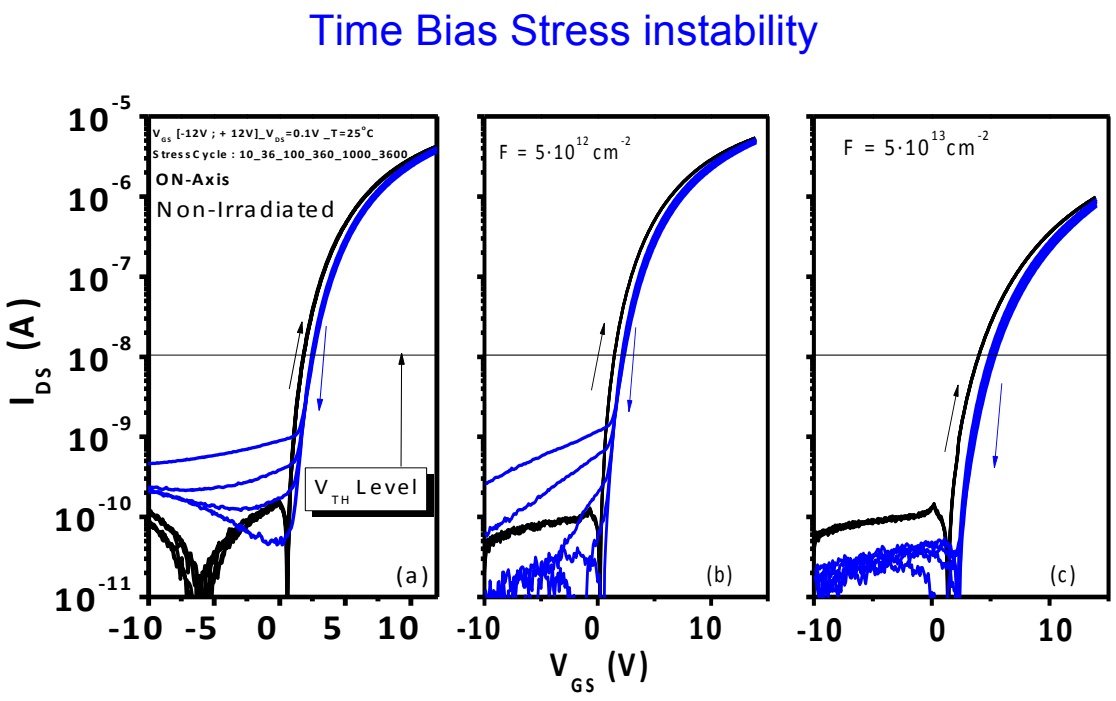


Fig C.6.45. Transconductance characteristic of MOSFETs (3) non-irradiated (a) and irradiated at 0.18 MeV with $5{\cdot}10^{12}$ cm^{-2} (b) and $5{\cdot}10^{13}$ cm^{-2} (c) proton fluence.

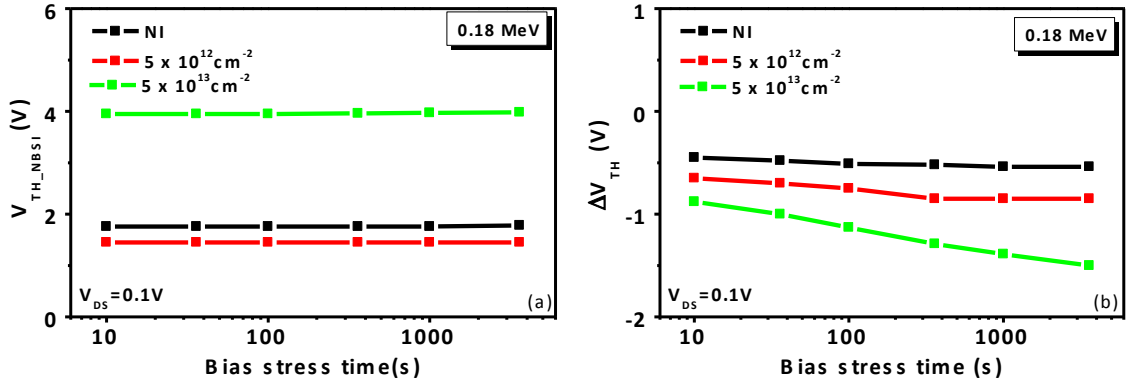


Fig C.6.46. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFETs (3) irradiated at 0.18 MeV.

C2) Post Irradiation annealing Data of 0.18 MeV of MOSFET (3)

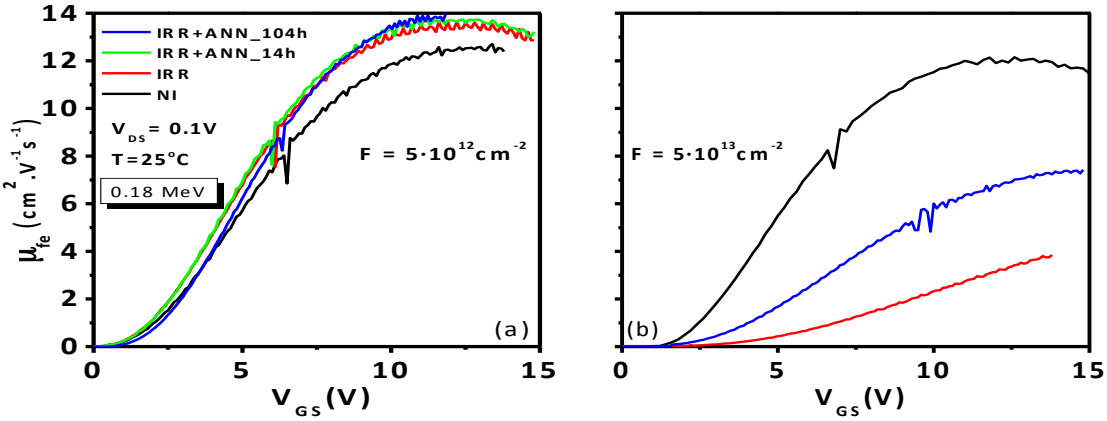


Fig C.6.47. The field effect mobility time evolution for 0.18 MeV proton irradiated MOSFET (3) at $5\cdot10^{12}$ cm^{-2} (a), $5\cdot10^{13}cm^{-2}$ (b) after irradiation and several time annealing (14h, 104h).

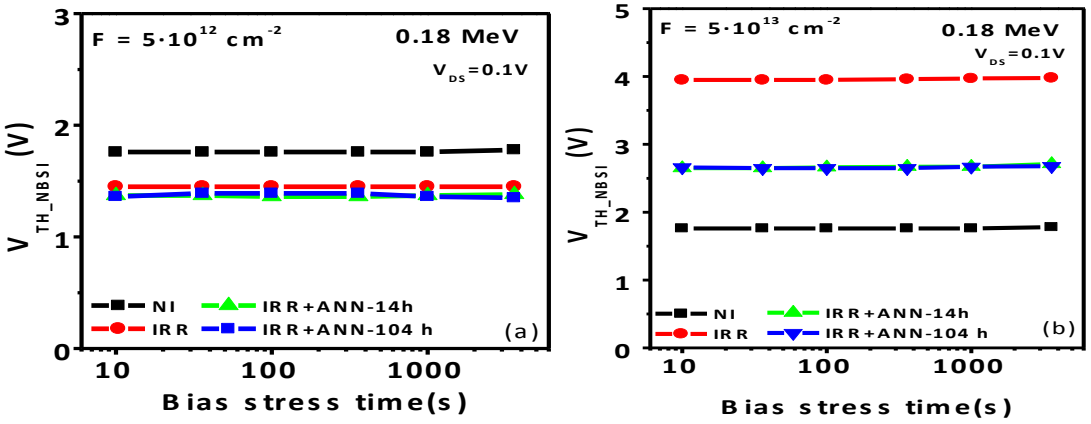


Fig C.6.48. The threshold voltage time evolution after a negative bias stress for 0.18 MeV proton irradiated MOSFETS (3) at $5\cdot10^{12}$ cm^{-2} (a) and $5\cdot10^{13}$ cm^{-2} (b) after irradiation and several post irradiation annealing time (14h, 104h).

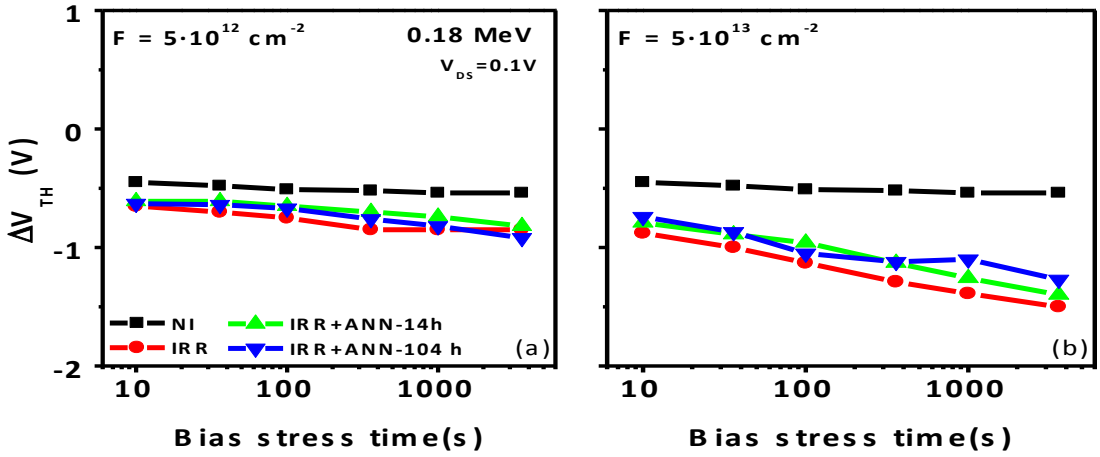


Fig C.6.49. The threshold voltage hysteresis time evolution after a 0.18 MeV proton irradiated MOSFETS (3) at $5\cdot10^{12}$ cm^{-2} (a), $5\cdot10^{13}$ cm^{-2} (b) after irradiation and several post irradiation annealing time (14h, 104h).

C3) Post irradiation annealing, temperature analysis data of 0.18 MeV of MOSFET (3)

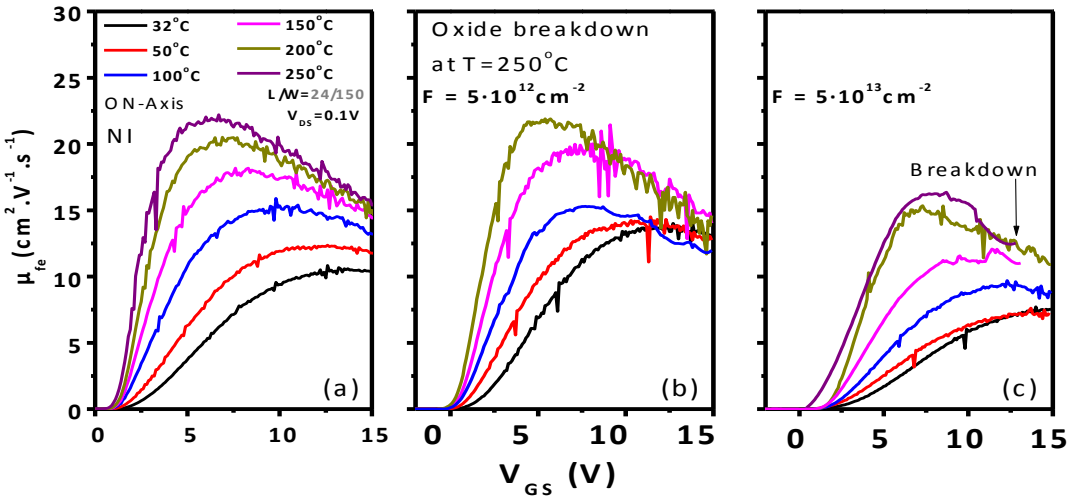


Fig C.6.50. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFETs (3) irradiated at 0.18 MeV with a proton dose of $5 \cdot 10^{12}$ cm^{-2} (b) and $5 \cdot 10^{13}$ cm^{-2} (c).

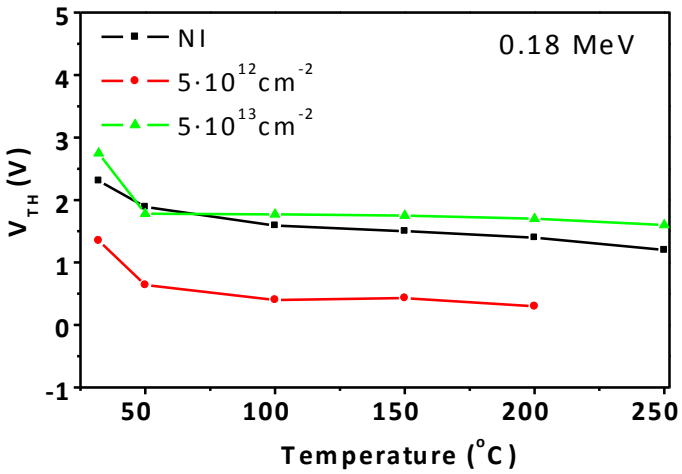


Fig C.6.51. The V_{TH} temperature evolution for the NI MOSFETs and post irradiation annealed MOSFETs (3) of all fluences and doses at a proton irradiation of 0.18 MeV.

C4) Irradiation Data of 10 MeV of MOSFET (3)

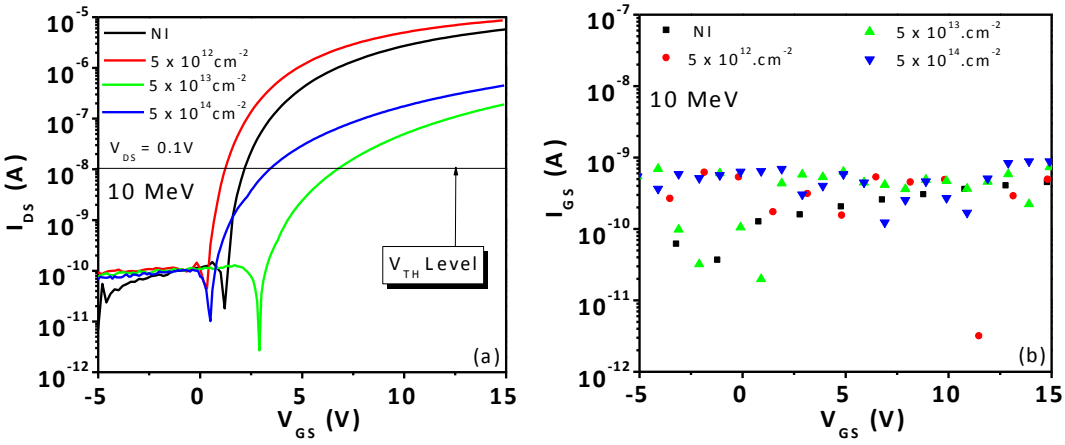


Fig C.6.52. Transconductance characteristics (a) and $I_{GS}(V_{GS})$ characteristics (b) of non-irradiated and irradiated MOSFET (3) at 10 MeV following different fluences ($5{\cdot}10^{12}$ cm^{-2}, $5{\cdot}10^{13}$ cm^{-2}, $5{\cdot}10^{14}$ cm^{-2}). All MOSFETs (3) contain an aluminum implanted well and its epilayer substrate is oriented on-axis.

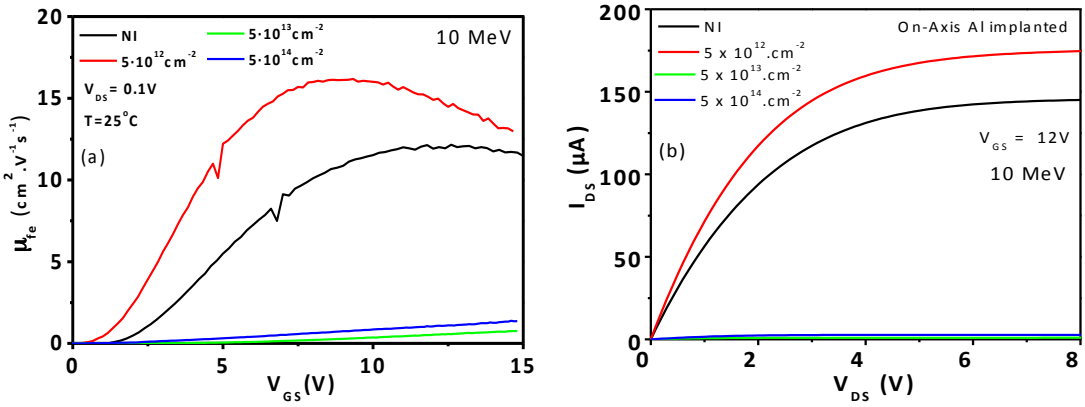


Fig C.6.53. μ_{fe} (V_{GS}) (a) and I_{DS} (V_{DS}) (b) of non-irradiated and irradiated MOSFETs (3) at 0.18 MeV following different fluences.

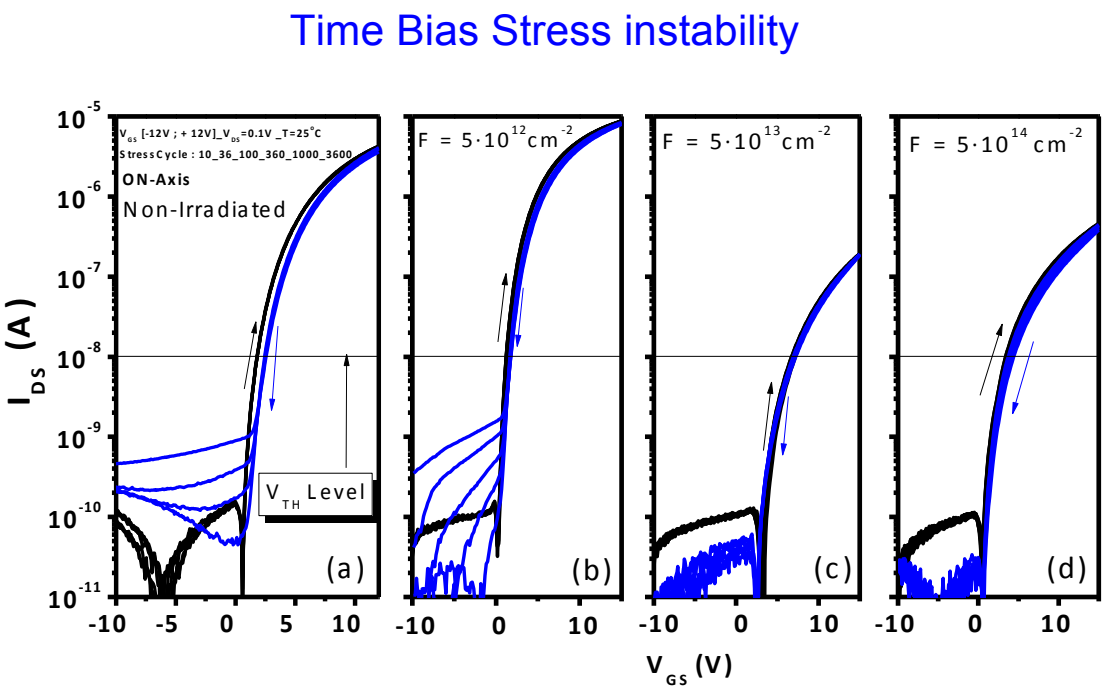


Fig C.6.54. BSI Transconductance characteristic of MOSFETs (3) non-irradiated (a) and irradiated at 10 MeV with $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c) and $5{\cdot}10^{14}$ cm^{-2} (d) proton fluences.

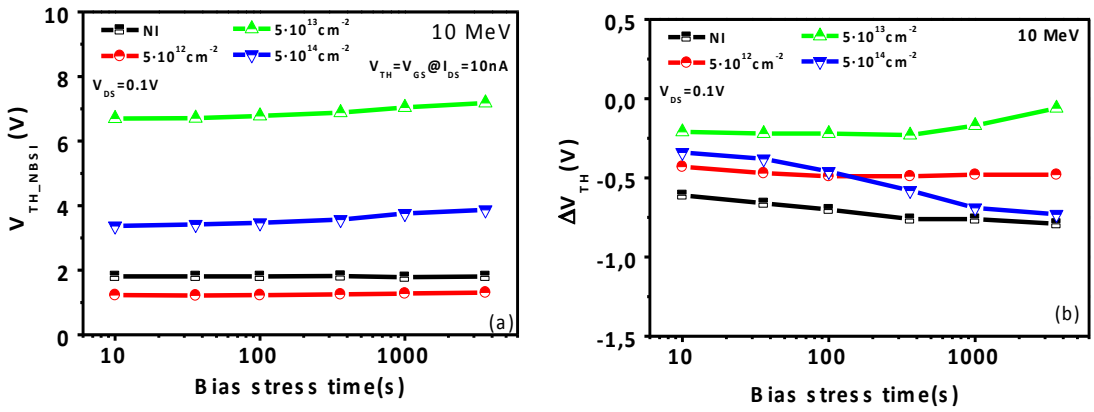


Fig C.6.55. Threshold voltage variation after a negative bias stress (V_{TH_NBSI}) with the time stress increase (a) and the threshold voltage hysteresis (ΔV_{TH}) (b) of MOSFETs (3) irradiated at 10 MeV.

C5) Post Irradiation annealing Data of 10 MeV of MOSFET (3)

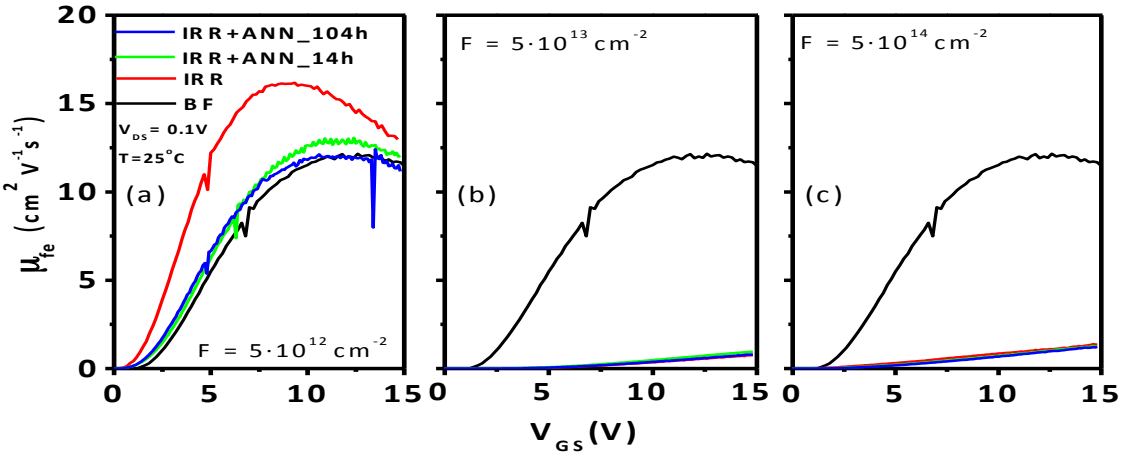


Fig 6.56. The field effect mobility time evolution for 10 MeV proton irradiated MOSFET (3) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$$cm^{-2}$ (b) and $5{\cdot}10^{14}$$cm^{-2}$ (c) after irradiation and several post irradiation annealing time.

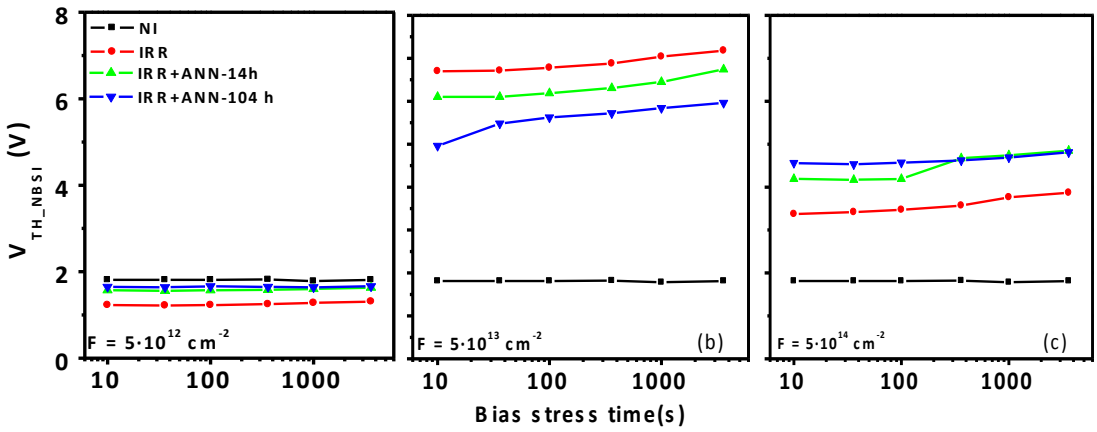


Fig C.6.57. The threshold voltage time evolution after a negative bias stress for 10 MeV proton irradiated MOSFETS (3) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

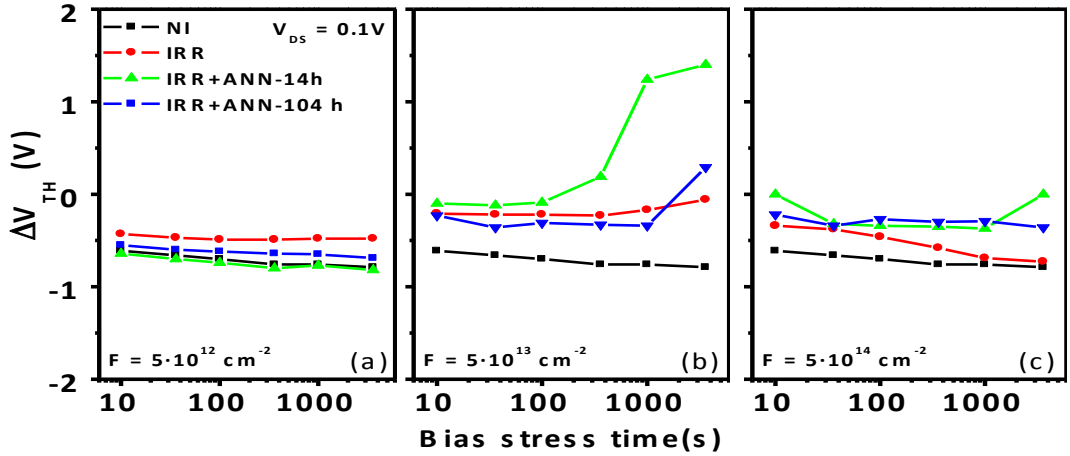


Fig C.6.58. The threshold voltage hysteresis time evolution after a 10 MeV proton irradiated MOSFETS (3) at $5{\cdot}10^{12}$ cm^{-2} (a), $5{\cdot}10^{13}$ cm^{-2} (b) and $5{\cdot}10^{14}$ cm^{-2} (c) after irradiation and several post irradiation annealing time (14h, 104h).

C6) Post irradiation annealing, temperature analysis data of 10 MeV of MOSFET (3)

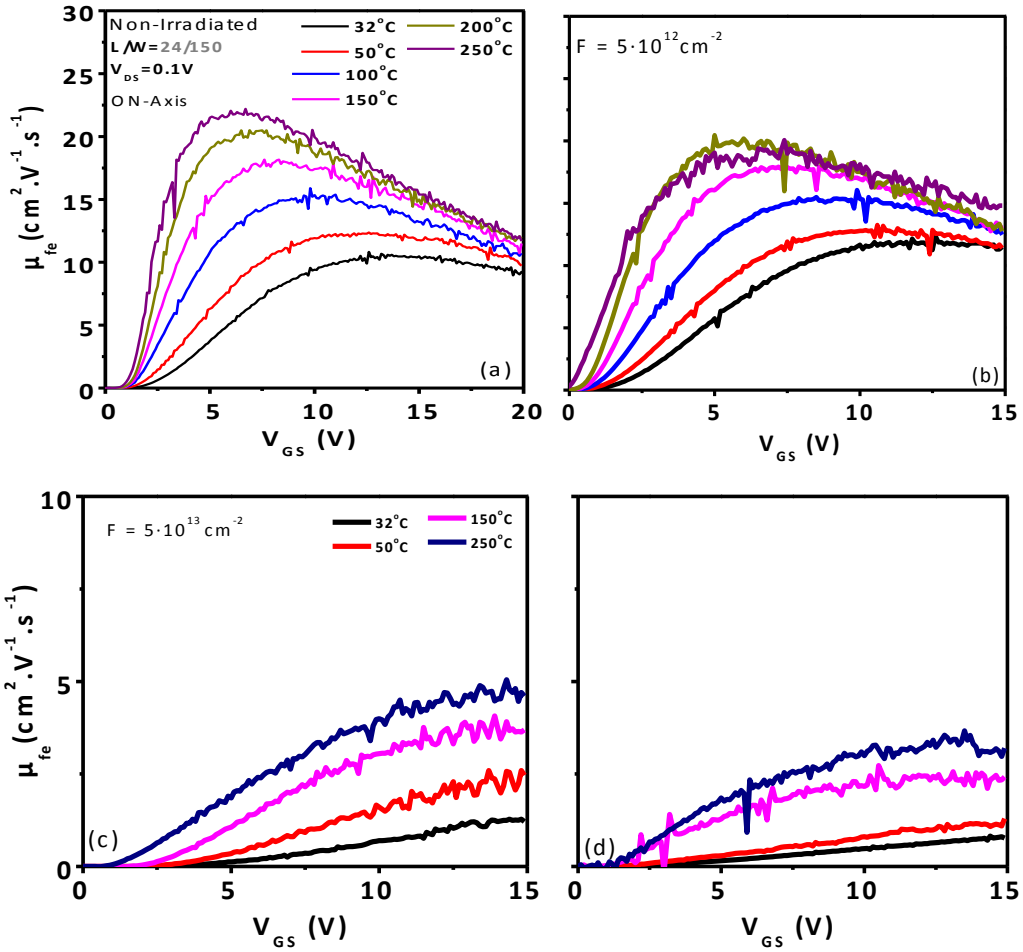


Fig C.6.59. Evolution of the μ_{fe} with the increase of temperature for non-irradiated (a) and post irradiation annealed MOSFETs irradiated at 10 MeV with a proton dose of $5{\cdot}10^{12}$ cm^{-2} (b), $5{\cdot}10^{13}$ cm^{-2} (c) and $5{\cdot}10^{14}$ cm^{-2} (d).

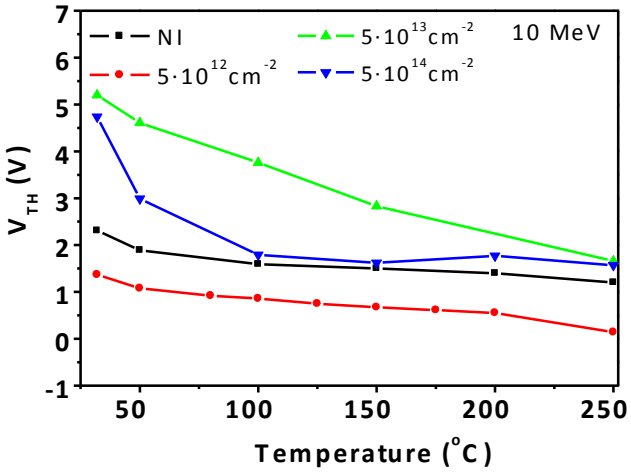


Fig C.6.60. The V_{TH} temperature evolution for the NI MOSFETs and post irradiation annealed MOSFETs (3) of all fluences and doses at a proton irradiation of 10 MeV.

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